The Sabre ES9821Q is a 32-bit analog-to-digital (A/D) converter targeted for professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW), test equipment, instruments, audio processors, digital turntables, and consumer applications.

The ES9821 has 2 integrated ADCs which use ESS' patented Hyperstream® II ADC Architecture, which delivers unprecedented audio sound quality and specifications, including a DNR of +120dB& THD+N of -112dB in 2 channel mode.

The SABRE® ADC supports S/PDIF, I2S master/slave, and TDM outputs, and Hardware mode for quick configurations.

The ES9821 has built-in preprogramed filter coefficients to match perfectly with the SABRE PRO Series of DACs including the ES9038PRO. These complimentary filters allow for analog-digital-analog processing with the upmost audio fidelity and minimized time-domain smearing.

The ES9821 has an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition, enabling higher resolution at higher sample rates.

Feature	Description
+120dB DNR per channelw/o PLL -112dB THD+N per channelw/o PLL	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Up to PCM 768kHz
Customizable filter characteristics	8 presets of digital optimal filters
Multiple Output formats available	PCM, TDM, and S/PDIF outputs are available
I2C, SPI, and Hardware interface control	Configured by microcontroller or other I2C/SPI master, or pins through Hardware Mode
Ultra-Low Noise Floor Bandwidth	200kHz bandwidth enabling higher resolution at higher sample rates
Integrated low noise ADC reference regulators	Reduced BOM cost, PCB area and improved DNR if required
Low Power Consumption	Simplifies power supply design
Low Pin Count Standardized Packaging	5mm x 5mm, 28 pin QFN

Applications

- Professional digital audio workstations Audio Recording
- Very high-quality microphones
- High quality record turntable to USB conversion

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Functional Block Diagram

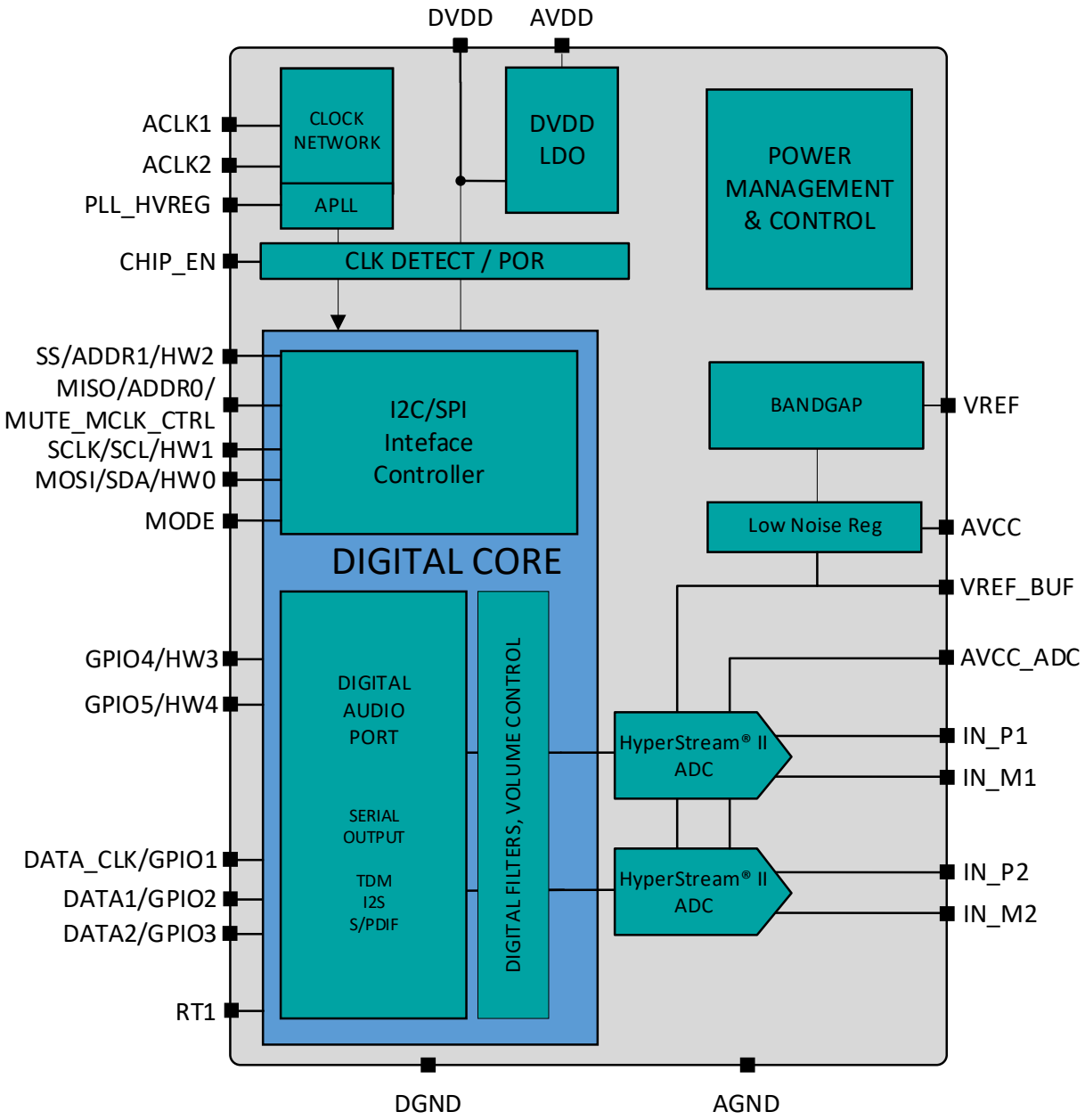


Figure 1 -ES9821Q Block Diagram

ES9821Q Package

28 QFN Pinout

(Pin 29 is QFN package pad, see package dimensions)

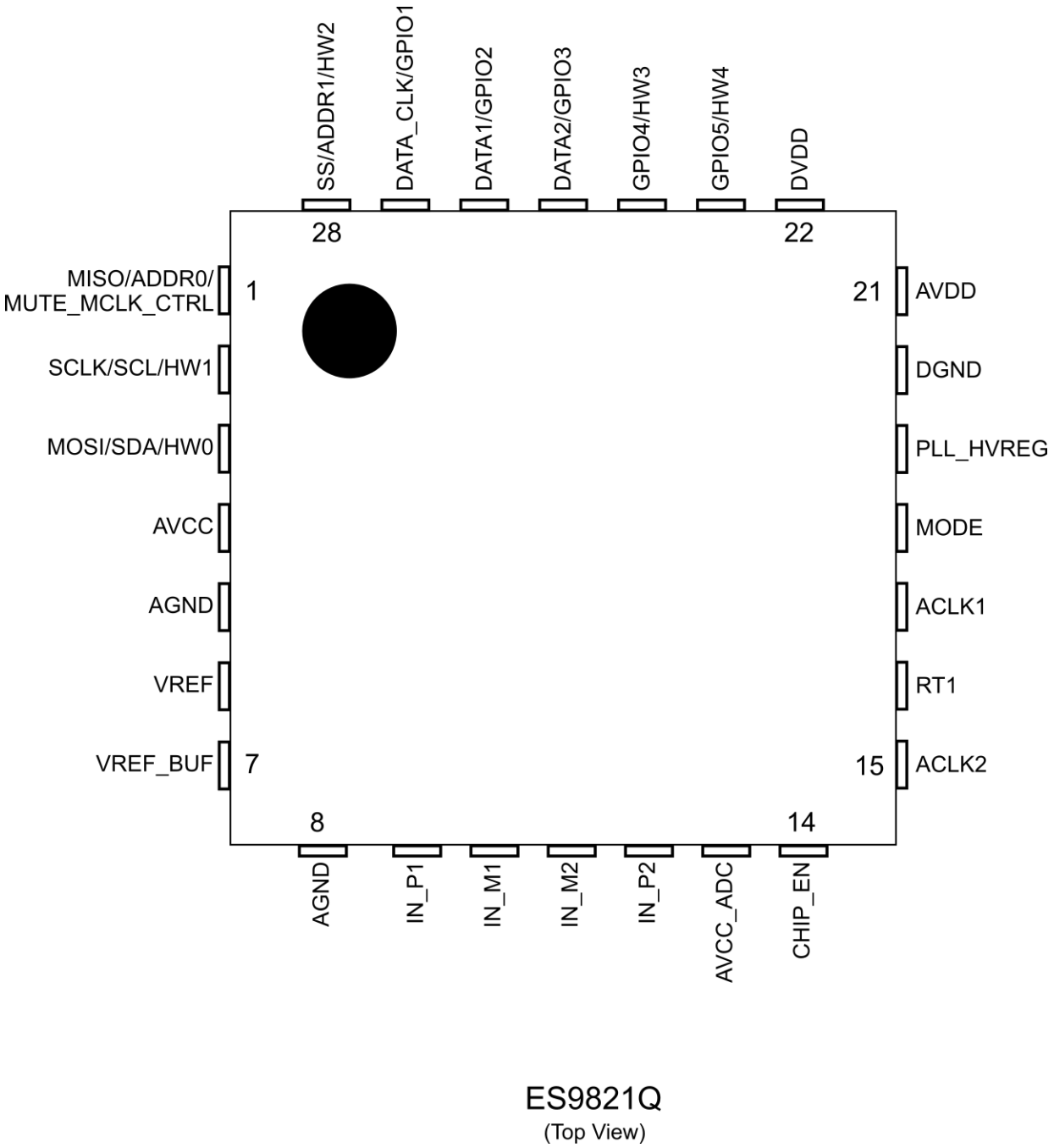


Figure 2 - 28 pin QFN pinout

Note: Pin 29 is a package pad, used for heat dissipation and is not electrically connected

28 QFN Pin List

Pin	Name	Pin Type	Reset State	Pin Description
1	MISO/ADDR0/MUTE_MCLK_CTRL	I/O	HiZ	Serial communication for SPI/I2C & HW interface pin, controlled by MODE pin
2	SCLK/SCL/HW1	I/O	HiZ	Serial Clock for SCLK (SPI), SCL (I2C), also HW1 controlled by MODE pin
3	MOSI/SDA/HW0	I/O	HiZ	Serial communication for SPI/I2C & HW0 interface pin, controlled by MODE
4	AVCC	Power	Power	3.3V Supply
5	AGND	Ground	Ground	Analog Ground
6	VREF	Power	Power	Low Noise reference for bandgap circuitry
7	VREF_BUF	Power	Power	Low Noise regulator output
8	AGND	Ground	Ground	Analog Ground
9	IN_P1	AI	HiZ	ADC Channel 1 differential positive (+) input
10	IN_M1	AI	HiZ	ADC Channel 1 differential negative (-) input
11	IN_M2	AI	HiZ	ADC Channel 2 differential negative (-) input
12	IN_P2	AI	HiZ	ADC Channel 2 differential positive (+) input
13	AVCC_ADC	Power	Power	ADC reference voltage 3.3V Supply
14	CHIP_EN	I/O	HiZ	Active-high chip enable.
15	ACLK2	AI	HiZ	Auxiliary Clock Input 2
16	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
17	ACLK1	AI	HiZ	Auxiliary Clock Input 1
18	MODE	I/O	HiZ	I2C/SPI Control selection or HW mode
19	PLL_HVREG	Power	Power	Low Noise reference for PLL regulator
20	DGND	Ground	Ground	Digital Core Ground
21	AVDD	Power	Power	3.3V, I/O Supply
22	DVDD	Power	Power	Digital Core Supply. Internally Supplied
23	GPIO5/HW4	I/O	HiZ	General I/O w/extended functions, HW4 mode control pin controlled by MODE
24	GPIO4/HW3	I/O	HiZ	General I/O w/extended functions, HW3 mode control pin controlled by MODE
25	DATA2/GPIO3	I/O	HiZ	Serial Data pin, also general I/O w/extended functions
26	DATA1/GPIO2	I/O	HiZ	Serial Data pin, also general I/O w/extended functions
27	DATA_CLK/GPIO1	I/O	HiZ	Serial Clock pin, also general I/O w/extended functions
28	SS/ADDR1/HW2	I/O	HiZ	Serial communication for SPI/I2C & HW2 interface pin, controlled by MODE pin
29*	Package PAD	-	-	Not electrically connected, used for heat dissipation

Table 1 - 28 QFN pin list

Note: Pin 29 is the package pad. See 28 QFN package dimensions for sizing. Connect to DGND if desired.

Hardware Mode

The ES9821 has pre-configured modes that can be set with external pin configuration. These modes configure the ADC for different serial data rates and set the ADC muting.

All Hardware modes use ACLK1, and use the default Minimum phase digital filter.

These modes are set with pins:

- MODE (pin 18)
- HW0 (pin 3)
- HW1 (pin 2)
- HW2 (pin 28)

Each hardware mode pin has 4 states:

- 0 – Pin directly connected to GND
- 1 – Pin directly connected to AVDD
- Pull 0 – Pin pulled to GND through 47kΩ resistor
- Pull 1 – Pin pulled to AVDD through 47kΩ resistor

Muting

MUTE_MCLK_CTRL (Pin 1) is used to control the muting of the output and MCLK rate while in Hardware Mode:

- 0 – Mute, 24.576MHz / 22.579MHz
- 1 – Unmuted, 24.576MHz / 22.579MHz
- Pull 0 – Mute, 49.152MHz / 45.158MHz
- Pull 1 – Unmuted, 49.152MHz / 45.158MHz

Hardware Mode Pin Configurations

HW Mode	FS (kHz)	BCK (MHz)	MCLK (MHz)	BCK/Channel	Channel Slots	MODE	HW2	HW1	HW0
	I2S Master Mode, Ext MCLK								
0	MCLK / 128	MCLK / 2	24.576/49.152	32	1,2	Pull 0	0	0	0
1	MCLK / 256	MCLK / 4	24.576/49.152	32	1,2	Pull 0	0	0	1
2	MCLK / 512	MCLK / 8	24.576/49.152	32	1,2	Pull 0	0	1	0
3	MCLK / 1024	MCLK / 16	24.576/49.152	32	1,2	Pull 0	0	1	1
	LJ Master, EXT MCLK (with SPDIF enabled on GPIO5)								
4	MCLK / 128	MCLK / 2	24.576/49.152	32	1,2	Pull 0	Pull 0	0	0
	LJ Master, Ext MCLK (with SPDIF enabled)								
5	MCLK / 256	MCLK / 4	24.576/49.152	32	1,2	Pull 0	Pull 0	0	1
6	MCLK / 512	MCLK / 8	24.576/49.152	32	1,2	Pull 0	Pull 0	1	0
7	MCLK / 1024	MCLK / 16	24.576/49.152	32	1,2	Pull 0	Pull 0	1	1
	I2S Slave, Ext MCLK, AutoDetect FS and BCK								
8	8 < FS < 384	64FS	24.576/49.152	32	1,2	Pull 0	Pull 1	0	0
	I2S Slave with PLL from BCK								
9	48	3.072	24.576 from PLL	32	1,2	Pull 0	Pull 1	0	1
10	96	6.144	24.576 from PLL	32	1,2	Pull 0	Pull 1	1	0
11	192	12.288	24.576 from PLL	32	1,2	Pull 0	Pull 1	1	1
	LJ Slave, AutoDetect FS and BCK								
12	8 < FS < 384	64FS	24.576/49.152	32	1,2	Pull 0	1	0	0
	LJ Slave with PLL from BCK								
13	48	3.072	24.576 from PLL	32	1,2	Pull 0	1	0	1
14	96	6.144	24.576 from PLL	32	1,2	Pull 0	1	1	0
15	192	12.288	24.576 from PLL	32	1,2	Pull 0	1	1	1
	TDM MSB Justified Slave, Autodetect FS and BCK								
16	8<FS<384	Auto (64FS, 128FS, 256FS, 512FS)	24.576/49.152	32	1,2	Pull 1	0	0	0
17	8<FS<384	Auto (64FS, 128FS, 256FS, 512FS)	24.576/49.152	32	3,4	Pull 1	0	0	1
18	8<FS<384	Auto (64FS, 128FS, 256FS, 512FS)	24.576/49.152	32	5,6	Pull 1	0	1	0
19	8<FS<384	Auto (64FS,	24.576/49.152	32	7,8	Pull 1	0	1	1

		128FS, 256FS, 512FS)							
20	8<FS<384	Auto (64FS, 128FS, 256FS, 512FS)	24.576/49.152	32	9,10	Pull 1	Pull 0	0	0
21	8<FS<384	Auto (64FS, 128FS, 256FS, 512FS)	24.576/49.152	32	11,12	Pull 1	Pull 0	0	1
22	8<FS<384	Auto (64FS, 128FS, 256FS, 512FS)	24.576/49.152	32	13,14	Pull 1	Pull 0	1	0
23	8<FS<384	Auto (64FS, 128FS, 256FS, 512FS)	24.576/49.152	32	15,16	Pull 1	Pull 0	1	1
	TDM MSB Justified Slave, Autodetect FS and BCK								
24	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	1,2	Pull 1	Pull 1	0	0
25	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	3,4	Pull 1	Pull 1	0	1
26	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	5,6	Pull 1	Pull 1	1	0
27	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	7,8	Pull 1	Pull 1	1	1
28	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	9,10	Pull 1	1	0	0
29	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	11,12	Pull 1	1	0	1
30	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	13,14	Pull 1	1	1	0
31	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	15,16	Pull 1	1	1	1
	TDM MSB Justified Slave, Autodetect FS and BCK								
32	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	17,18	Pull 1	0	0	0
33	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	19,20	Pull 1	0	0	1

34	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	21,22	Pull 1	0	1	0
35	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	23,24	Pull 1	0	1	1
36	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	25,26	Pull 1	Pull 0	0	0
37	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	27,28	Pull 1	Pull 0	0	1
38	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	29,30	Pull 1	Pull 0	1	0
39	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	32	31,32	Pull 1	Pull 0	1	1
	TDM MSB Justified Slave, Autodetect FS and BCK								
40	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	17,18	Pull 1	Pull 1	0	0
41	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	19,20	Pull 1	Pull 1	0	1
42	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	21,22	Pull 1	Pull 1	1	0
43	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	23,24	Pull 1	Pull 1	1	1
44	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	25,26	Pull 1	1	0	0
45	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	27,28	Pull 1	1	0	1
46	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	29,30	Pull 1	1	1	0
47	8<FS<384	Auto (32FS, 64FS, 128FS, 256FS)	24.576/49.152	16	31,32	Pull 1	1	1	1

Table 2 - Hardware mode configurations

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted. If using a PLL mode, the device should be set to hardware mode 8 (HW2 pulled high, and HW0-1 set low) before CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode is finalized, then asserted last.

Without PLL (Modes 0-8, 12):

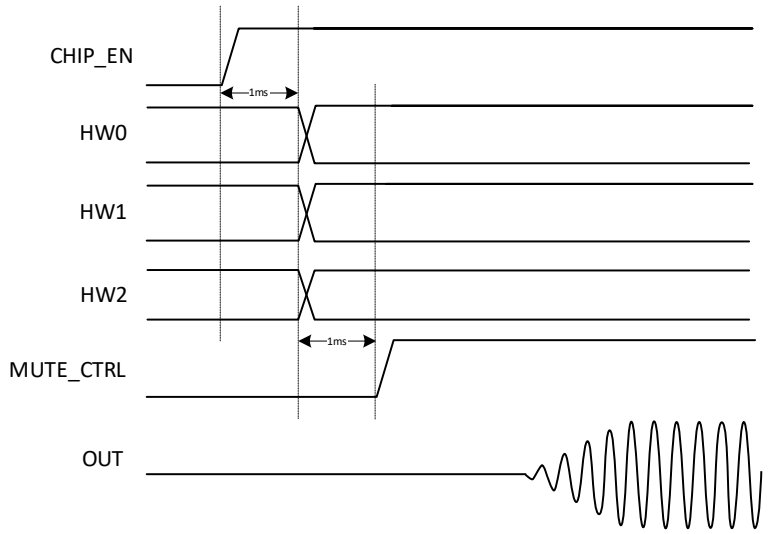


Figure 3 - hardware mode startup sequence for modes without PLL

With PLL (Modes 9-11, 13-15):

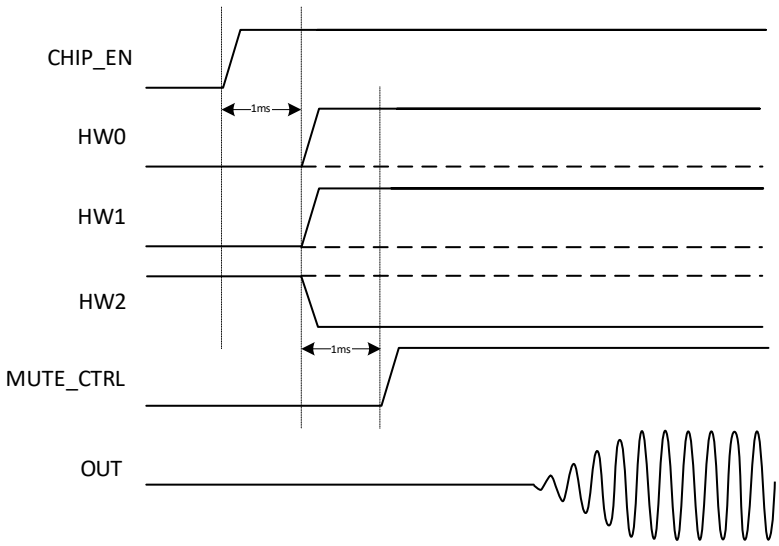


Figure 4 - hardware mode startup sequence for modes with PLL

Software Mode

The registers for the ES9821Q can be accessed either using an I²C or SPI interface.

The MODE pin (pin 18) determines which interface will be used.

I²C

- MODE (Pin 18) – ***GND***
- Connect per I²C standard
  - SDA (Pin 3)
  - SCL (Pin 2)
  - ADDR0 (Pin 1)
  - ADDR1 (Pin 28)
- ADDR1 & ADDR2 determine the I²C address
  - I²C Slave Address = [5'b00100,ADDR2,ADDR1]
    - Possible addresses are 0x40, 0x42, 0x44, and 0x46 for I²C slave address
  - I²C Slave Address = [5'b00100,ADDR2,ADDR1]
    - Possible addresses are 0x48, 0x4A, 0x4C, and 0x4E for I²C synchronous slave address

Available I2C Addresses for the ES9821Q:

I2C Slave Address	I2C Synchronous Slave Address	ADDR1	ADDR0
0x40	0x48	***GND***	***GND***
0x42	0x4A	***GND***	***AVDD***
0x44	0x4C	***AVDD***	***GND***
0x46	0x4E	***AVDD***	***AVDD***

Table 3 - Available I2C addresses

I²C Slave Interface (Device Address 0x40,0x42,0x44,0x46)

This interface contains Read/Write and Read-only registers. A system clock must be present.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.

MSB is always stored in the highest register address.

Read/Write Register Addresses

Registers 0–65 (0x00 – 0x41) are read/write registers

Read-only Register Addresses

Registers224 – 240 (0xE0 – 0xF0) are read only registers.

I²C Synchronous Slave Interface (Device Address 0x48,0x4A,0x4C,0x4E)

This interface contains Write-only registers. These registers can be written even when there is no system clock present.

When the device is inactive, all peripherals are automatically disabled and all clocks are stopped. An interrupt or a reset can wake the ES9821Q

Write-only Register Addresses

Registers192 – 204 (0xC0 – 0xCC) are write only registers.

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

MSB is always stored in the highest register address.

I²C Slave/Synchronous Slave Interface Timing

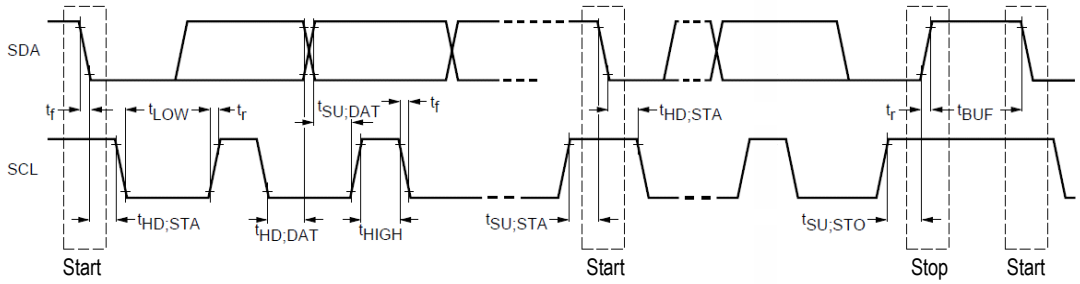


Figure 5 - I2C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	<CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 4 - I2C Slave Control Interface Timing definitions

SPI

The SPI slave interface is used when the MODE pin (pin 18) is pulled high.

- Mode (Pin 18) – **AVDD**
- Connect per SPI standard using pins 1-3, and 28
  - SCLK (Pin 2)
  - SS (Pin 28)
  - MOSI (Pin 3)
  - MISO (Pin 1)

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

SPI Commands

- 0x01: Read
- 0x03: Write
- 0x07: Write-only Register Addresses 192-194 (0xC0 – 0xC2)

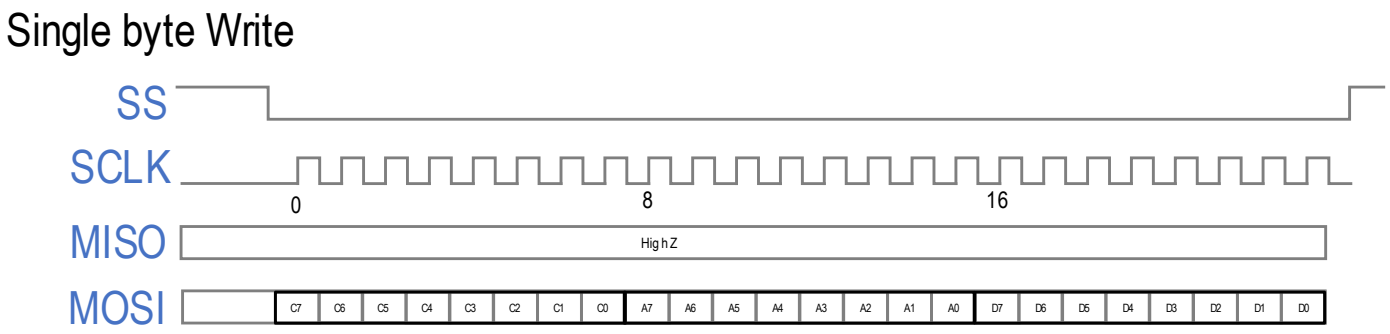


Figure 6 - SPI single byte write

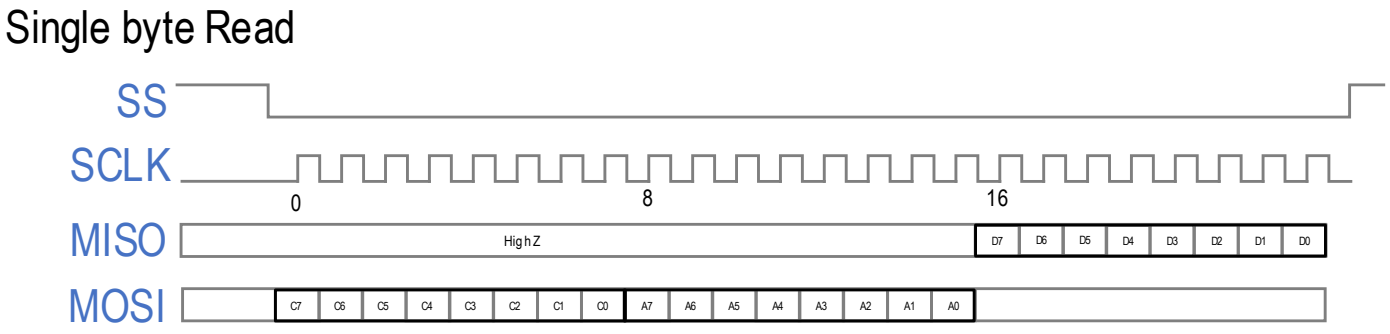


Figure 7 - SPI single byte Read

Multi-byte Read

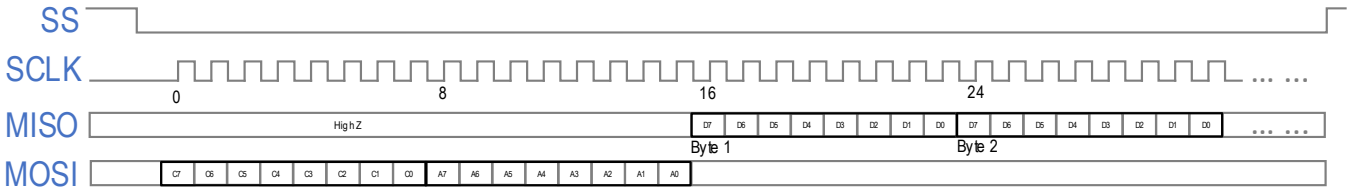


Figure 8 - SPI multi-byte read

Digital Features

Digital Signal Path

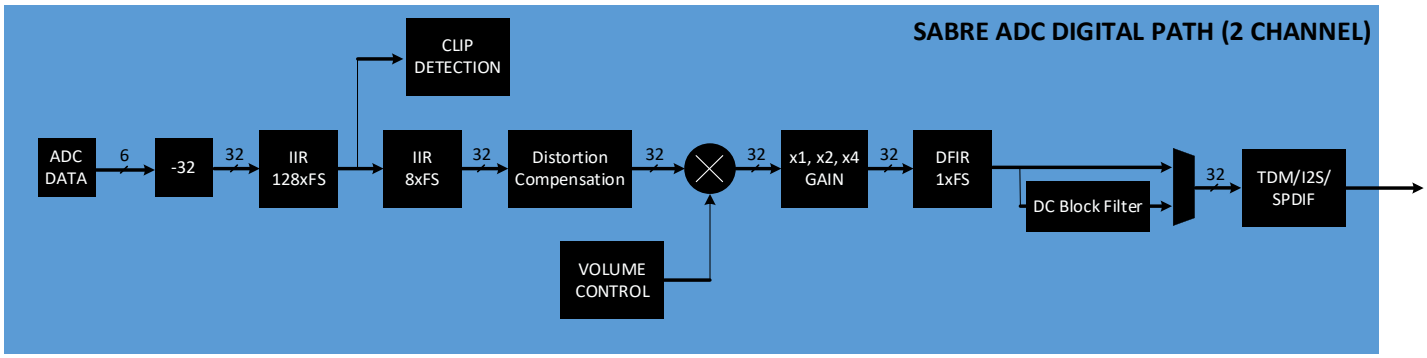


Figure 9 - Digital signal path

GPIO Configuration

gpio#_config	function	I/O Direction
0	analog shutdown	Shutdown (default)
1	Aux Inputs	Inputs
2	Aux Outputs	Output
3	PLL_CLK_AVALID	Output
4	PLL_LOCKED	Output
5	Ch1_CLIP_INTERRUPT	-
6	Ch2_CLIP_INTERRUPT	-
7	INTERRUPT (OR of all interrupts)	-
8	SPDIF data output	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
12	RESERVED	Output
13	CLK ADC	Output
14	1'b0	Output
15	1'b1	Output

Table 5 – Standard GPIO Functions

Note: GPIOs can be configured using registers 26-31.

For configuring pins as inputs, outputs, or Input/Outputs:

- Input pin
  - GPIOxx_IE = 1'b1 (Input Enable), Registers 31-29
  - GPIOxx_OE = 1'b0 (Output Enable), Registers 31-29
- Output pin
  - GPIOxx_IE = 1'b0
  - GPIOxx_OE = 1'b1
- In/Out pin (Master Mode)
  - GPIOxx_IE = 1'b1
  - GPIOxx_OE = 1'b1

  In Master mode GPIO1 & GPIO 2 should be configured as In/Out pins

Interrupts

Interrupts are enabled using individual configuration registers specific to the interrupt function. For example, the Peak Detection interrupt is enabled via Register 43 *ADC_PEAK_DETECTOR_CONFIG*.

Once set, interrupts must be manually cleared via Register 12 *INTERRUPT*.

Register 12 *INTERRUPT* also allows for masking of the interrupt flag bits in Register 224 *READ_SYSTEM_REGISTER_0*.

Interrupts can be mapped to GPIO pins using Registers 26-28 *GPIO_x/x_CONFIG*.

THD Compensation

THD Compensation minimizes the non-linearities of the ADCs

The ES9821Q can help compensate for system second and third harmonic distortion.

THD compensation is always enabled but if register values are zero, it will be bypassed

- *Register 56-55, THD COMP C2 CH1*
- *Register 58-57, THD COMP C3 CH1*
- *Register 60-59, THD COMP C2 CH2*
- *Register 62-61, THD COMP C3 CH2*

For best results, compensation coefficients should be tuned for each device in-situ.

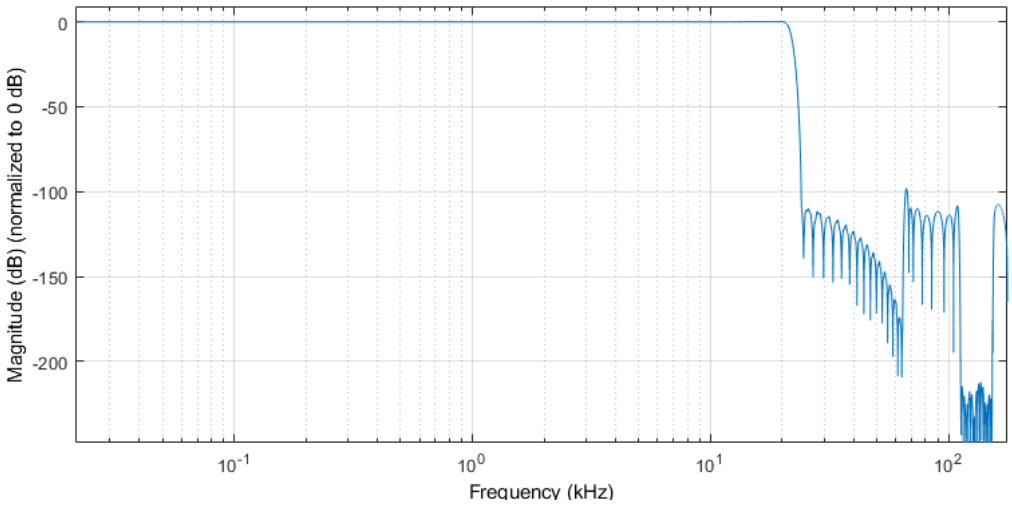
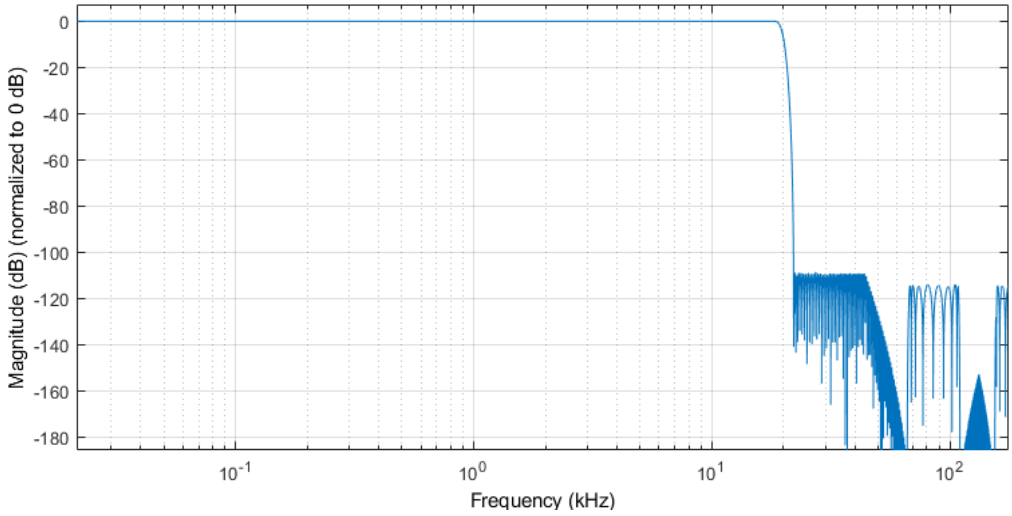
Pre-Programmed Digital Filters

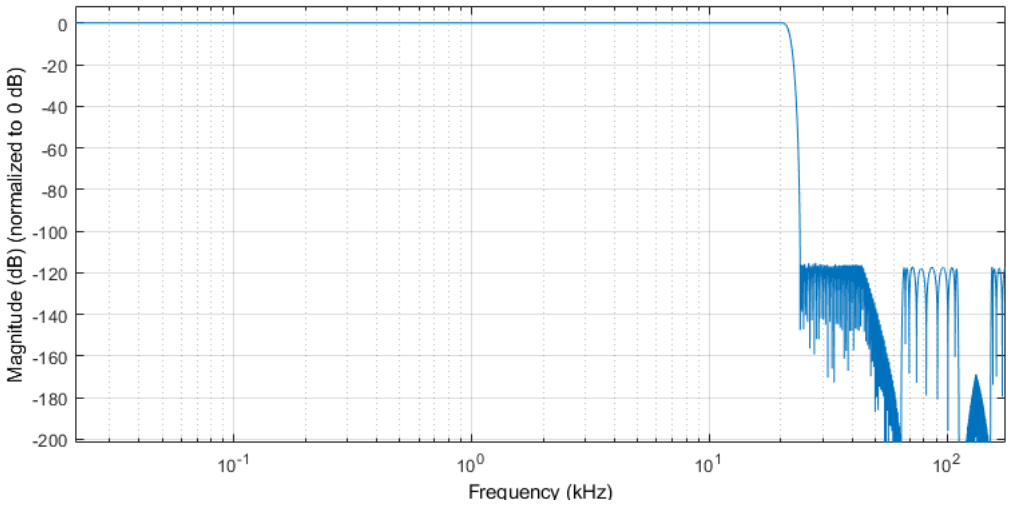
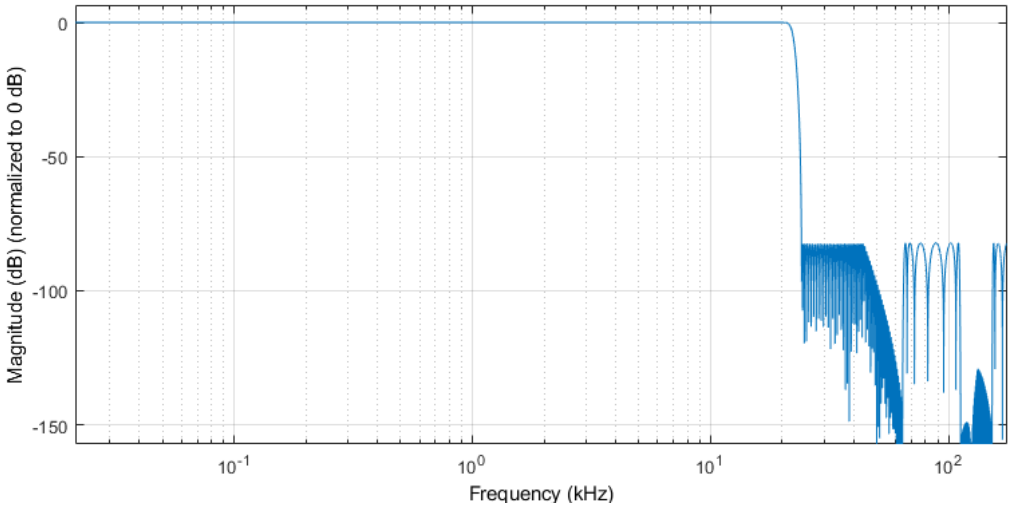
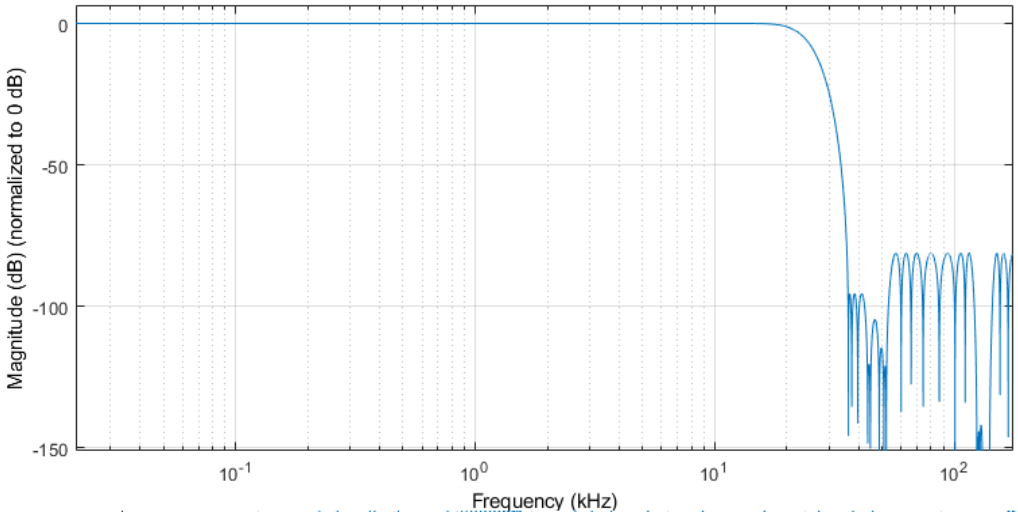
The ES9821 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates.

- Minimum phase (default)
- Linear phase apodizing
- Linear phase fast roll-off
- Linear phase fast roll-off low ripple
- Linear phase slow roll-off
- Minimum phase fast roll-off
- Minimum phase slow roll-off low dispersion

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-off	
Linear Phase Fast Roll-off Low Ripple	
Linear Phase Slow Roll-off	

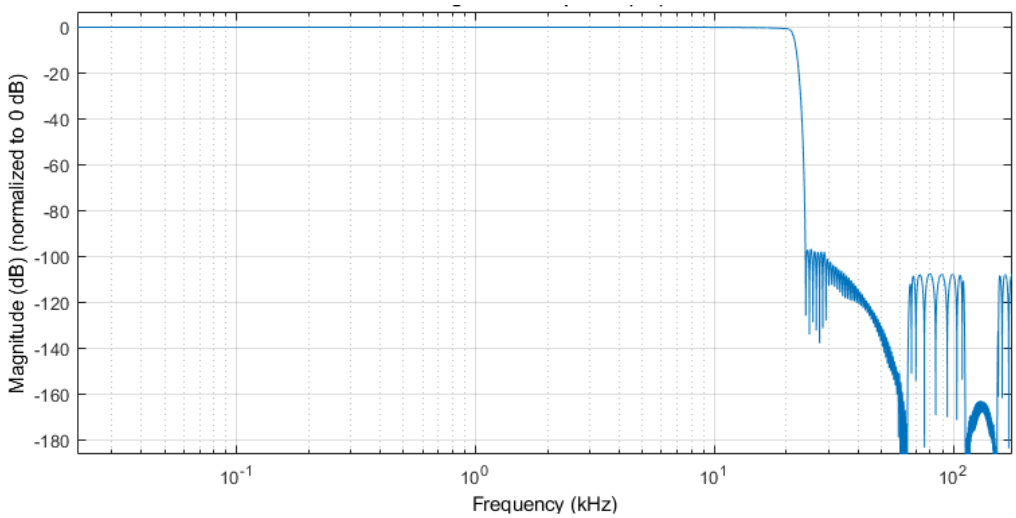
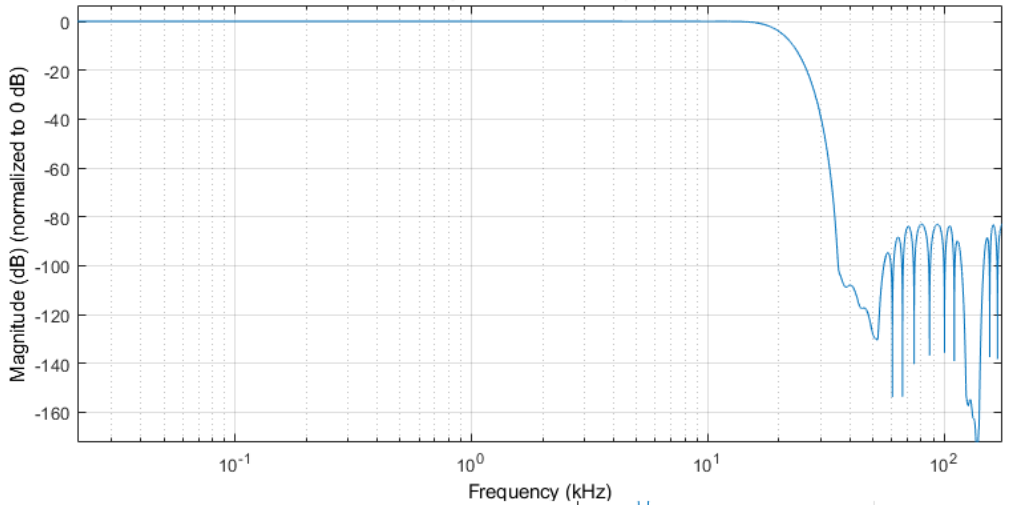
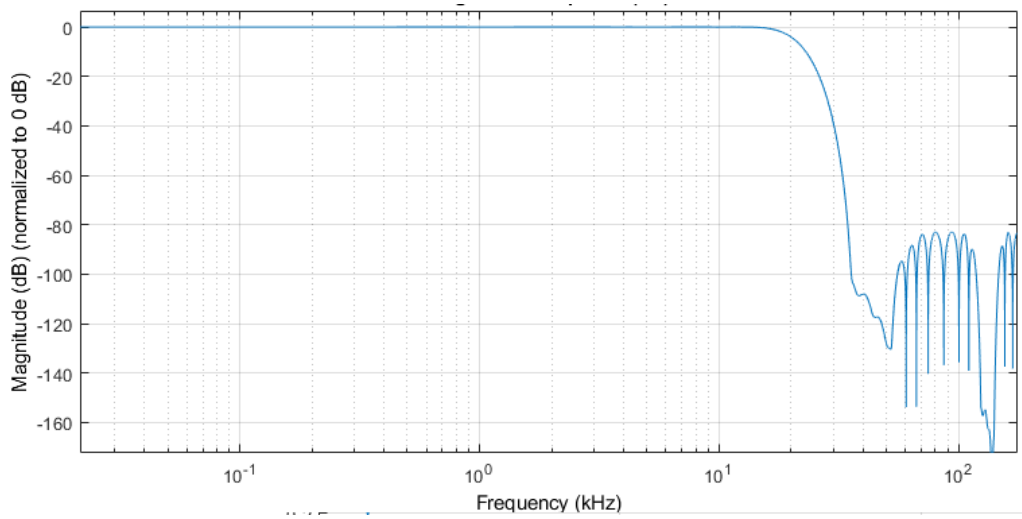
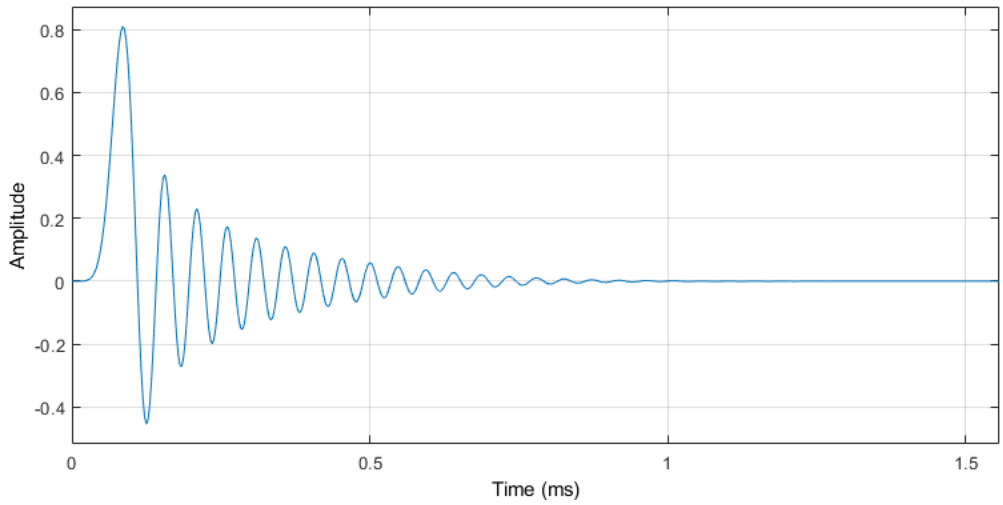
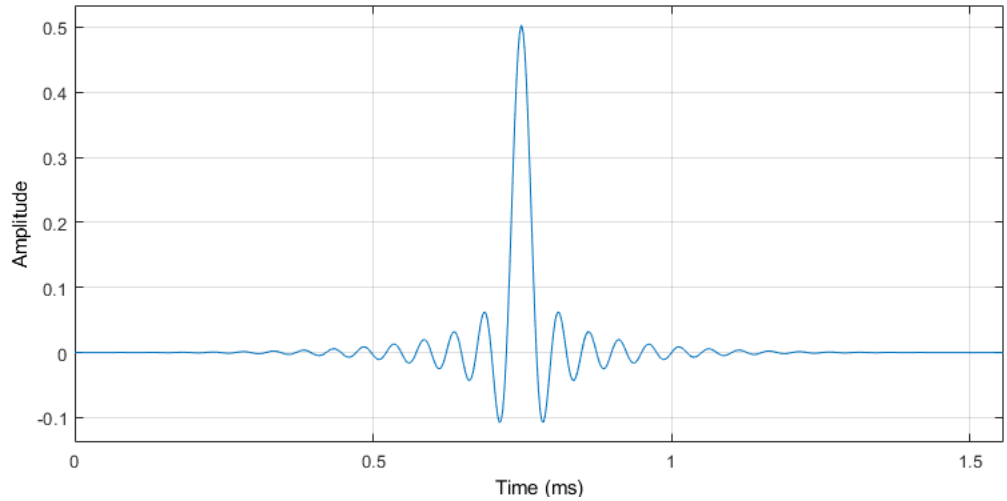
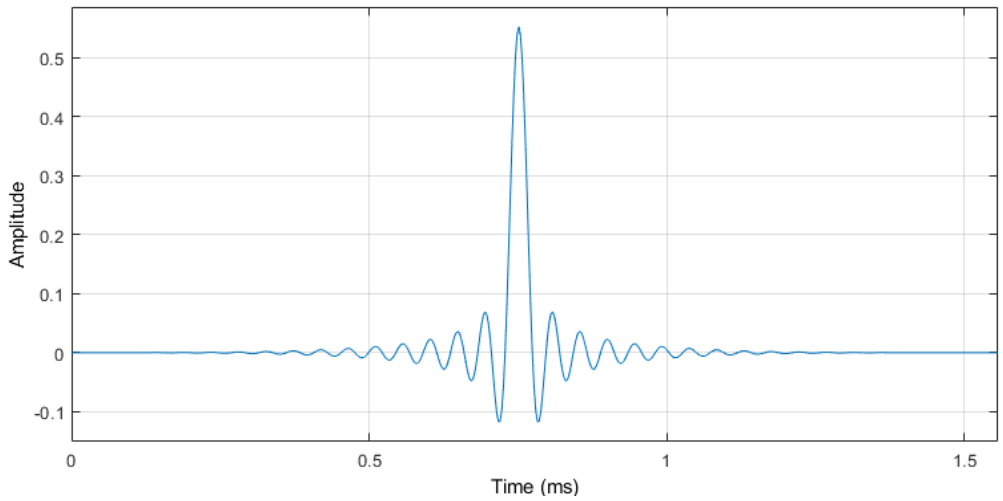
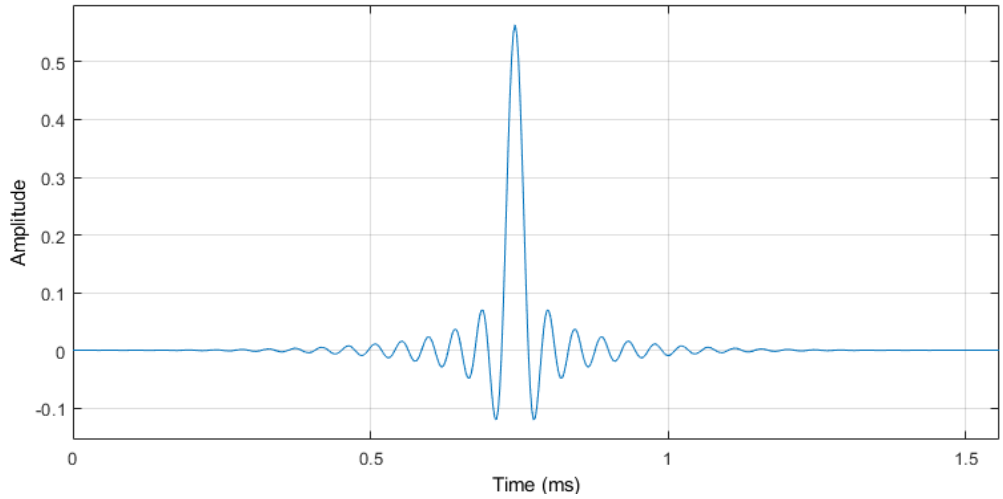
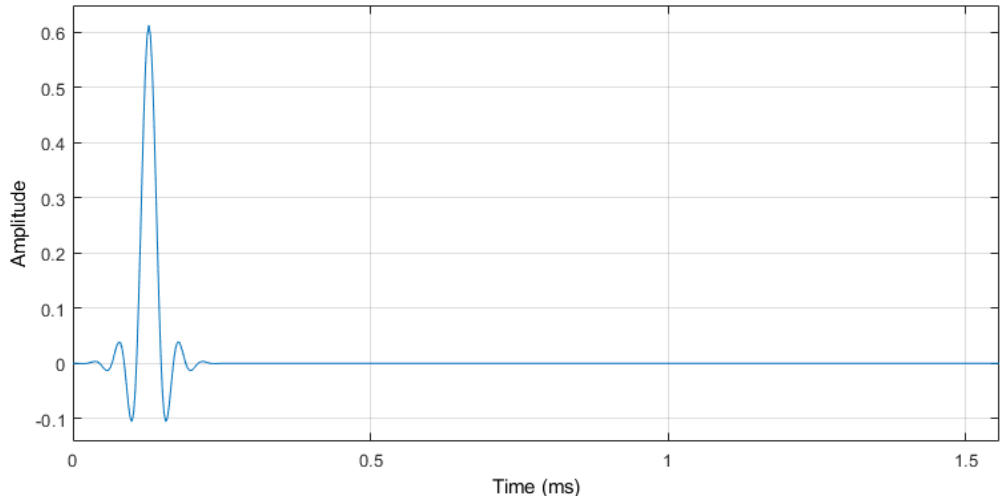
Minimum Phase Fast Roll-off	
Minimum Phase Slow Roll-off	
Minimum Phase Slow Roll-off Low Dispersion	

Table 6 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-off	
Linear Phase Fast Roll-off Low Ripple	
Linear Phase slow roll-off	

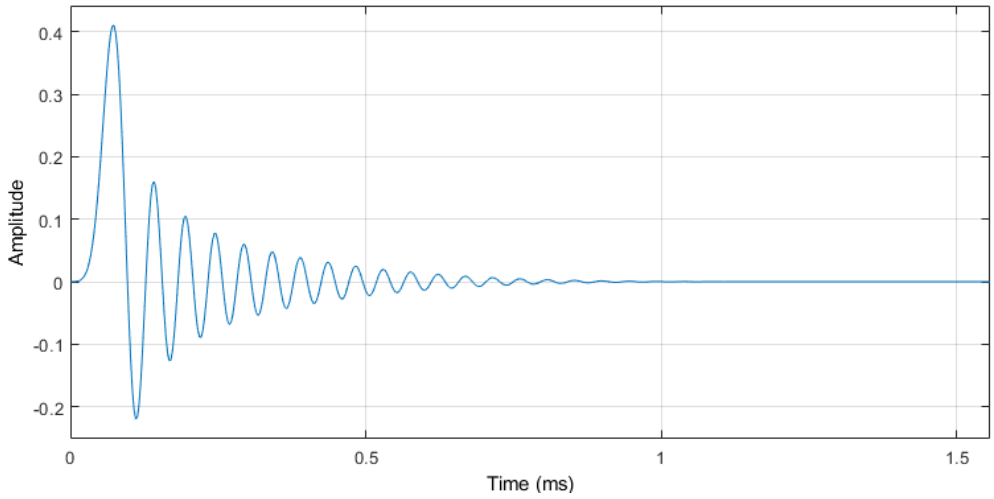
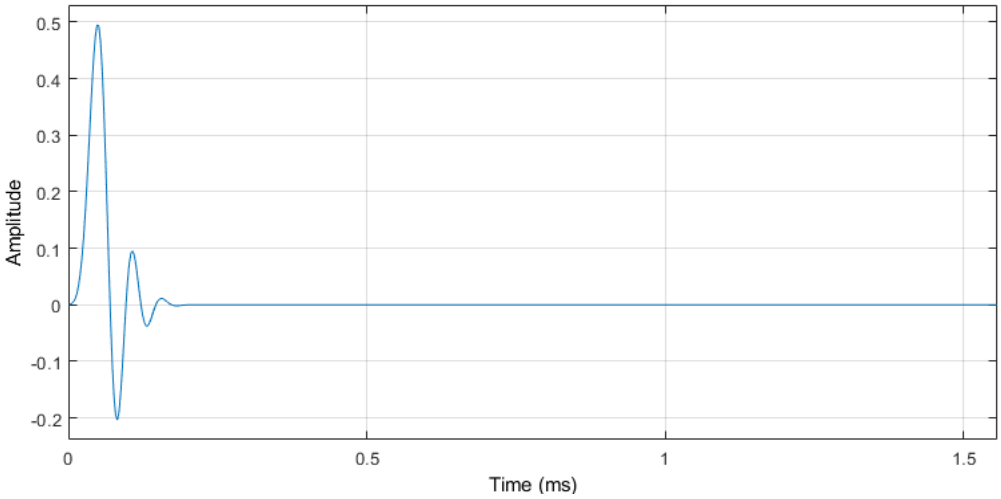
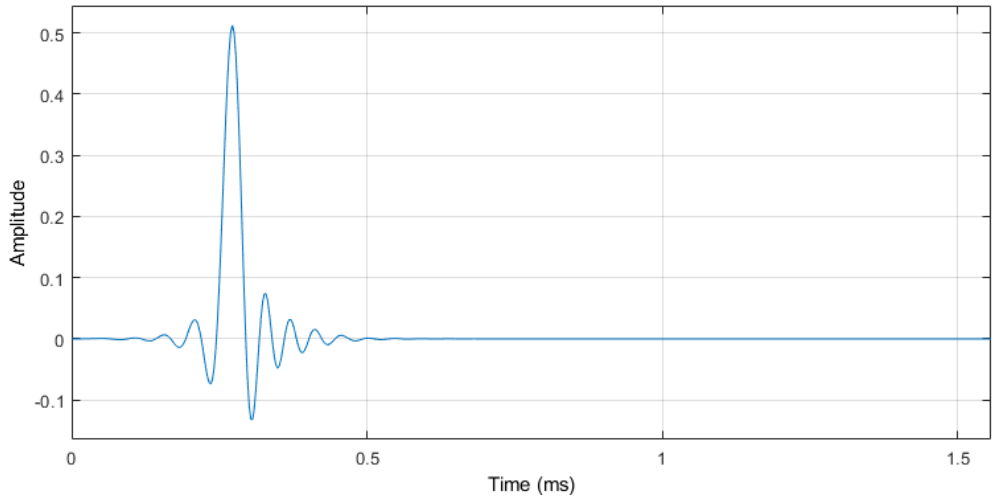
Minimum phase fast roll-off	
Minimum phase slow roll-off	
Minimum phase slow roll-off low dispersion	

Table 7 - PCM Filter Impulse Response

Clock Distribution

The ES9821 includes features for selecting and manipulating the input clock source.

The minimum MCLK frequency is 22.5792MHz.

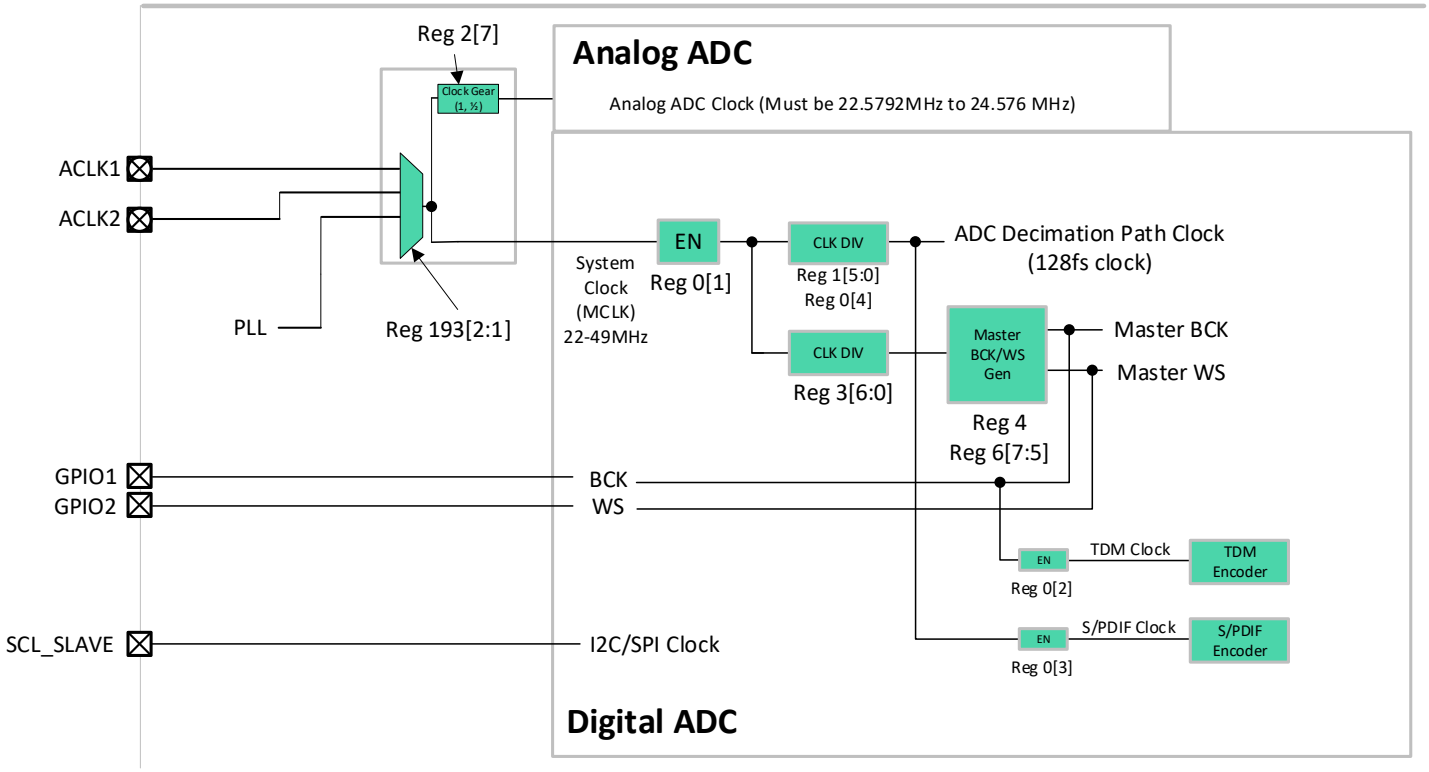


Figure 10 - ES9821Q Clock Distribution

The following list shows the various clocks of the ES9821 and the associated registers for configuration.

Analog ADC Clock

ADC clock must be maintained to be between 22.5792MHz & 24.576MHz

- Reg 194[0] (SEL_CLK_DIV)
- Reg 193[2:1] (SEL_SYSCLK_IN)
- Reg 193[0] (EN_ANA_CLKIN)

ADC Decimation Path Clock

- Reg 2[4:0] (SELECT_ADC_NUM)
- Reg 1
    - Dependent on channels 1 & 2
- Reg 9[6:0]
- Reg 193[2:1] (SEL_SYSCLK_IN)
- Reg 193[0] (EN_ANA_CLKIN)

Master BCK&WS

- Reg 8
- Reg 7[7:5] MASTER_WS_SCALE
- Reg 9[6:0] SELECT_I2S_TDM_NUM
- Reg 193[2:1] (SEL_SYSCLK_IN)
- Reg 193[0] (EN_ANA_CLKIN)

TDM Clock

- Reg 10[0] (ENABLE_TDM_CLK)

S/PDIF Clock

- Reg 5[2] (ENABLE_SPDIF_CLK)

I2S Master Clock Rate Configurations

WS can be scaled down further than shown via Register 6 [7:5] *MASTER_WS_SCALE*.

When enabling 16-bit mode, the following registers must be modified:

- Register 63 [0:1] – enable 16-bit mode on channels 1 and 2
- Register 5 [0] – set TDM length to 16-bits
- Register4[5:4] – set master frame length to 16-bits

MCLK Frequency	WS [kHz]	BCK [MHz]	Bits	Channels	Register 1 [5:0] SELECT_ADC_NUM		Register 3 [6:0] SELECT_I2S_TDM_NUM	
					value	divider	value	divider
22.579 MHz	44.1	2.822	32	2	5'd3	4	7'd3	4
	88.2	5.645		2	5'd1	2	7'd1	2
	176.4	11.290		2	5'd0	1	7'd0	1
	44.1	1.411	16	2	5'd3	4	7'd3	4
	88.2	2.822		2	5'd1	2	7'd1	2
	176.4	5.645		2	5'd0	1	7'd0	1
24.576 MHz	48	3.072	32	2	5'd3	4	7'd3	4
	96	6.144		2	5'd1	2	7'd1	2
	192	12.288		2	5'd0	1	7'd0	1
	48	1.536	16	2	5'd3	4	7'd3	4
	96	3.072		2	5'd1	2	7'd1	2
	192	6.144		2	5'd0	1	7'd0	1
45.158 MHz	44.1	2.822	32	2	5'd7	8	7'd7	8
	88.2	5.645		2	5'd3	4	7'd3	4
	176.4	11.290		2	5'd1	2	7'd1	2
	352.8	22.579		2	5'd0	1	7'd0	1
	44.1	1.411	16	2	5'd7	8	7'd7	8
	88.2	2.822		2	5'd3	4	7'd3	4
	176.4	5.645		2	5'd1	2	7'd1	2
	352.8	11.290		2	5'd0	1	7'd0	1
49.152 MHz	48	3.072	32	2	5'd7	8	7'd7	8
	96	6.144		2	5'd3	4	7'd3	4
	192	12.288		2	5'd1	2	7'd1	2
	384	24.576		2	5'd0	1	7'd0	1
	48	1.536	16	2	5'd7	8	7'd7	8
	96	3.072		2	5'd3	4	7'd3	4
	192	6.144		2	5'd1	2	7'd1	2
	384	12.288		2	5'd0	1	7'd0	1

Table 8 - I2S Master Clock Rate Configurations

I2S Slave Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK	Channels	Register 1 [5:0] SELECT_ADC_NUM		Register 0 [4] ENABLE_2X_MODE	
				value	divider	value	multiplier
22.579 MHz	44.1	512FS	2	7'd3	4	1'b0	1x
	88.2	256FS	2	7'd1	2	1'b0	1x
	176.4	128FS	2	7'd0	1	1'b0	1x
	352.8	64FS	2	7'd0	1	1'b1	2x
24.576 MHz	48	512FS	2	7'd3	4	1'b0	1x
	96	256FS	2	7'd1	2	1'b0	1x
	192	128FS	2	7'd0	1	1'b0	1x
	384	64FS	2	7'd0	1	1'b1	2x
45.158 MHz	44.1	1024FS	2	7'd7	8	1'b0	1x
	88.2	512FS	2	7'd3	4	1'b0	1x
	176.4	256FS	2	7'd1	2	1'b0	1x
	352.8	128FS	2	7'd0	1	1'b0	1x
49.152 MHz	48	1024FS	2	7'd7	8	1'b0	1x
	96	512FS	2	7'd3	4	1'b0	1x
	192	256FS	2	7'd1	2	1'b0	1x
	384	128FS	2	7'd0	1	1'b0	1x

Table 9 - I2S Slave Clock Rate Configurations

Digital Audio Output Port

Pins are configured in Master (AUX Output) or Slave (Aux Input) modes through GPIO Configurations.

PCM Pin Connections

See Audio Interface Timing (I2S) for timing criteria. Can select GPIO 4-6 for the datapath.

Pin Name	Function	Description
GPIO1/DATA_CLK	I2S BCLK	I2S clock (Master or Slave)
GPIO2/DATA1	I2S WS	I2S WS (Master or Slave)
GPIO3/DATA2	I2S DATA	I2S DATA out (selectable for 2 channels)

Table 10 - PCM pin connections

TDM Pin Connections

See Registers 7-15 for configuration, Can select GPIO 4-6 for the datapath.

Pin Name	Function	Description
GPIO1/DATA_CLK	TDM BCK	TDM clock (Master or Slave)
GPIO2/DATA1	TDM WS	TDM WS (Master or Slave)
GPIO3/DATA2	TDM DATA	TDM DATA out (default)

Table 11 - TDM pin connections

S/PDIF Pin Connections

S/PDIF Output is provided on GPIOs. Use GPIOx_CFG for S/PDIF output.

Pin Name	Description
GPIOx	GPIOx_CFG setting for GPIO of 4'd8 (S/PDIF output)

Table 12 - S/PDIF pin connections

AnalogFeatures

APLL

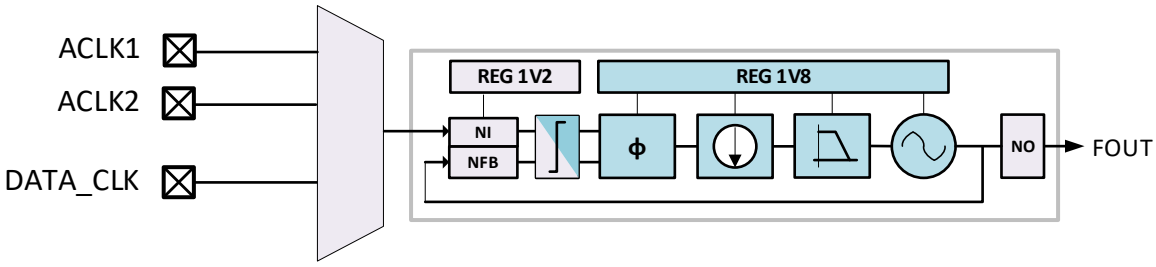


Figure 11 - Functional Block Diagram of ES9821 APLL

The ES9821Q has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally.

For calculation of the PLL frequency output, use the following formula:

$$Fout = \left(\frac{FIN}{NI}\right) * \frac{NFB}{NO}$$

$$NFB = \frac{(2^{25})}{FBDIV}$$

Where:

a. FBDIV is a 24-bit number
b. Fvco = Fout * NO, where Fvco must be between 90MHz and 100MHz
c. NI = input dividing ratio,
   - Accessible from Reg 202-200[9:1], **PLL_CLK_IN_DIV**
d. NO = output dividing ratio
   - Accessible from Reg 202-200[18:10], **PLL_CLK_OUT_DIV**
e. NFB = feedback dividing ratio,
   - Accessible from Reg 199-197[23:0], **PLL_CLK_FB_DIV**

PLL Registers

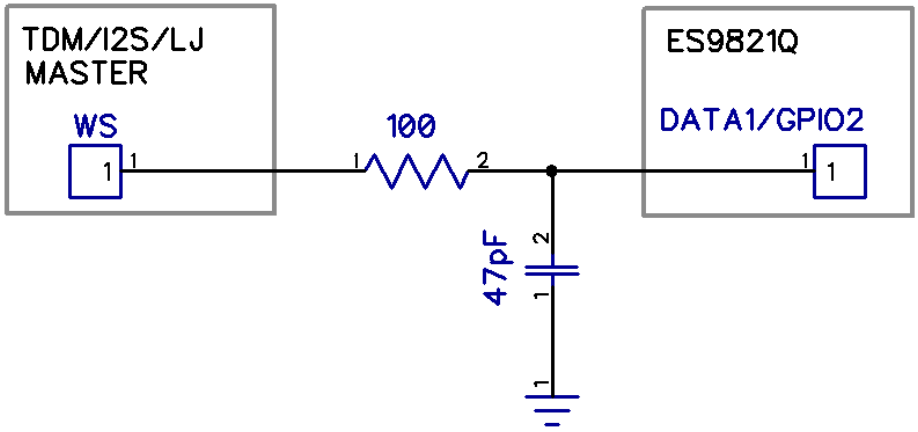
- NI – Register 200-202[9:1] PLL_CLK_IN_DIV
- NO – Register 200-202[18:10] PLL_CLK_OUT_DIV
- FBDIV – Register 197-199[23:0] PLL_CLK_FB_DIV

Clock Selection

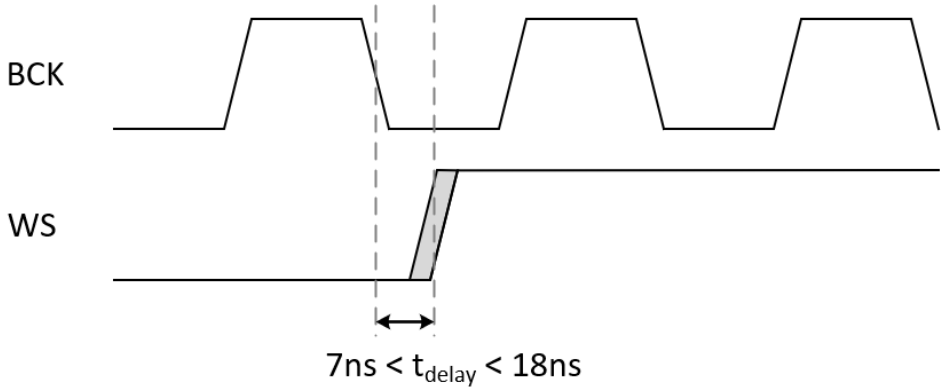
- SEL_PLL_IN – Register 194[5:4]
  - Selection of PLL clock source (ACLK1/ACLK2/BCK or DATA_CLK)
- SEL_PLL_CLKIN – Register 194[3]
  - Enables SEL_PLL_IN source input
- SEL_SYSCLK_IN – Register 194[2:1]
  - Selection of the ADC & digital core clock (ACLK1/ACLK2/PLL)

Note: 45-49MHz system clock is not supported when using the PLL in software mode.Use a 22-24MHz input clock, and gives a maximum sample rate of 384kHz.

If the PLL usage is a requirement in the ES9821Q, a RC circuit is required on DATA1/GPIO1.



To synchronize the input data with the MCLK domain the edge of the frame clock (WS/DATA1) is used. This can lead to a possible timing issue if the BCK and WS edges align leading to a condition where the clock can no longer be synchronized at low temperatures (<5ºC)



If the audio clock (TDM/I2S/LJ) source meets the timing requirements outlined above, no action is necessary. Otherwise, the delay may be implemented by adding a RC network between the WS (DATA1) source and the ES9821Q input pin using a 100Ω/47pF combination.

The RC circuit was verified on the EVB and provided stable operation at all PLL sample rates (48kHz-192kHz) across the supported temperature ranges.

Note: When installing the RC circuit, the PLL_CLK_PHASE bit must be set (1'b1) in SW mode. This bit is cleared by default (1'b0). In hardware mode, this bit is always set.

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_R/AVCC_L • AVCC • AVDD • DVDD	 • +3.6V with respect to Ground • +3.6V with respect to Ground • +3.6V with respect to Ground • +1.4V with respect to Ground
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD (nom) + 0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 13 - Absolute maximum ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	(AVDD / 2) + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD–0.2		V	IOH = ((AVDD / 2) +1.4) mA
Low-level output voltage	VOL		0.2	V	IOL = ((AVDD / 2) + 1.7) mA

Table 14 - IO electrical characteristics

Recommended Operating Conditions

There are the recommended operating conditions for the ES9821.

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +85°C
AVCC		3.3V
AVCC_ADC		3.3V
AVDD		3.3V
VREF		Internal
VREF_BUF		Internal
DVDD		Internal
Input DC offset		AVCC/2

Table 15 - Recommended operating conditions

Note: The minimum acceptable MCLK is 22MHz. Below this frequency, the device will not function.

Power Consumption

Test Conditions (unless otherwise noted)

T_A = 25°C, AVCC = AVCC_ADC = AVDD = +3.3V, fs = 48kHz, **MCLK = 49.152MHz**, I2S output, with -1dBFS output signal

MCLK of 49.152Mhz will work for all sample rates

Parameter	Min	Typ	Max	Unit
Supply Current during 48kHz 2ch mode				
AVCC		6.4		mA
AVCC_ADC		3.8		mA
AVDD		13		mA
Standby (CHIP_EN = LOW)				
AVCC + AVCC_ADC		6		uA
AVDD		<1		uA

Table 16–49.152MHz MCLK power consumption

Performance

Test Conditions (unless otherwise noted)

T_A = 25°C, AVCC = AVCC_ADC= AVDD = +3.3V, fs = 48kHz, MCLK = 49.152MHz, I2S output

Measurements were done usingESS Evaluation Board (EVB)

Parameter			Min	Typ	Max	Unit
Resolution				32		Bit
0dBFS Input Voltage(differential)				2		Vrms
THD+N Ratio (w/o PLL) @ fs=48kHz, BW=20Hz-20kHz	2 ch mode	-1dBFS		-112	-109	dB
THD+N Ratio (w/ PLL) @ fs=48kHz, BW=20Hz-20kHz				-106	-102	
DNR A-weighted (w/o PLL)	2ch mode	-60dBFS	117	120		dB
DNR A-weighted (w/ PLL)			106	110		
Interchannel Gain Mismatch				±0.05	±0.1	dB

Table 17 - Performance test results

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	RESERVED		ENABLE_ 2X_MODE	ENABLE_SPDIF _ENCODE	ENABLE_ TDM_ENCODE	ENABLE_ ADC_REG	RESERVED
0x01	1	ADC CLOCK CONFIG1	AUTO_ CH_DETECT	SELECT_ ADC_HALF	SELECT_ADC_NUM					
0x02	2	ADC CLOCK CONFIG2	ADC_CLK_DIV2	RESERVED			SELECT_ IADC_HALF	SELECT_IADC_NUM		
0x03	3	I2S/TDM MASTER CLK CONFIG	SELECT_I2S_ TDM_HALF	SELECT_I2S_TDM_NUM						
0x04	4	I2S/TDM MASTER MODE CONFIG	MASTER_ BCK_DIV1	MASTER_ WS_IDLE	MASTER_FRAME_LENGTH		MASTER_WS_ PULSE_MODE	MASTER_ BCK_INVERT	MASTER_ WS_INVERT	MASTER_ MODE_ ENABLE
0x05	5	TDM CONFIG1	RESERVED					TDM_ VALID_EDGE	TDM_LJ	TDM_LENGTH
0x06	6	TDM CONFIG2	MASTER_WS_SCALE			TDM_CH_NUM				
0x07	7	TDM SLOT CONFIG CH1	RESERVED		SLAVE_BCK_ INVERT	TDM_SLOT_SEL_CH1				
0x08	8	TDM SLOT CONFIG CH2	RESERVED			TDM_SLOT_SEL_CH2				
0x09 - 0x0B	9 - 11	RESERVED	RESERVED							
0x0C	12	INTERRUPT	RESERVED		INTERRUPT_CL EAR_CH2_CLIP _DETECTION	INTERRUPT_CL EAR_CH1_CLIP _DETECTION	RESERVED		INTERRUPT_M ASK_CH2_CLIP _DETECTION	INTERRUPT_M ASK_CH1_CLIP _DETECTION
0x0D	13	SPDIF CONFIG	SPDIF_CS							
0x0E	14	SPDIF CONFIG	SPDIF_CS							
0x0F	15	SPDIF CONFIG	SPDIF_CS							
0x10	16	SPDIF CONFIG	SPDIF_CS							
0x11	17	SPDIF CONFIG	SPDIF_CS							
0x12 - 0x19	18 - 25	RESERVED	RESERVED							
0x1A	26	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x1B	27	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x1C	28	GPIO5 CONFIG	GPIO5_READ	RESERVED			GPIO5_CFG			
0x1D	29	GPIO CONFIGS	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x1E	30	GPIO CONFIGS	INVERT_GPIO1	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN	GPIO5_SDB	GPIO4_SDB
0x1F	31	GPIO CONFIGS	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2
0x20	32	PWM1 COUNT	PWM1_COUNT							
0x21	33	PWM1 FREQUENCY	PWM1_FREQ							
0x22	34	PWM1 FREQUENCY	PWM1_FREQ							
0x23	35	PWM2 COUNT	PWM2_COUNT							
0x24	36	PWM2 FREQUENCY	PWM2_FREQ							
0x25	37	PWM2 FREQUENCY	PWM2_FREQ							
0x26	38	PWM3 COUNT	PWM3_COUNT							
0x27	39	PWM3 FREQUENCY	PWM3_FREQ							
0x28	40	PWM3 FREQUENCY	PWM3_FREQ							
0x29	41	ADC DATAPATH CONTROL	RESERVED	ADC_BYPASS_ FIR2X	ADC_BYPASS_ FIR4X	RESERVED			CH1_AVR	MONO_MODE
0x2A	42	ADC DC BLOCKING & SCALE CONFIG	ADC_DATA_SCALE_CH2		ADC_DATA_SCALE_CH1		ADC_SELECT_ DC_BLOCKING _CH2	ADC_SELECT_ DC_BLOCKING _CH1	ADC_ENABLE_ DC_BLOCKING _CH2	ADC_ENABLE_ DC_BLOCKING _CH1
0x2B	43	ADC PEAK DETECTOR CONFIG	ADC_ LOCK_PEAK	ADC_DECAY_RATE					ADC_ENABLE_ PEAK_DETECT	ADC_ENABLE_ PEAK_DETECT

								_CH2	_CH1
0x2C	44	ADC CH1 PEAK DETECTOR LEVEL	ADC_CLIP_LEVEL_CH1						
0x2D	45	ADC CH2 PEAK DETECTOR LEVEL	ADC_CLIP_LEVEL_CH2						
0x2E	46	ADC CH1 DC OFFSET	ADC_CH1_DC_OFFSET						
0x2F	47	ADC CH1 DC OFFSET	ADC_CH1_DC_OFFSET						
0x30	48	ADC CH2 DC OFFSET	ADC_CH2_DC_OFFSET						
0x31	49	ADC CH2 DC OFFSET	ADC_CH2_DC_OFFSET						
0x32	50	ADC CH1 VOLUME	ADC_CH1_VOLUME						
0x33	51	ADC CH1 VOLUME	ADC_CH1_VOLUME						
0x34	52	ADC CH2 VOLUME	ADC_CH2_VOLUME						
0x35	53	ADC CH2 VOLUME	ADC_CH2_VOLUME						
0x36	54	ADC VOLUME RATE	ADC_VOLUME_RATE						
0x37	55	THD COMP C2 CH1	THD_C2_CH1						
0x38	56	THD COMP C2 CH1	THD_C2_CH1						
0x39	57	THD COMP C3 CH1	THD_C3_CH1						
0x3A	58	THD COMP C3 CH1	THD_C3_CH1						
0x3B	59	THD COMP C2 CH2	THD_C2_CH2						
0x3C	60	THD COMP C2 CH2	THD_C2_CH2						
0x3D	61	THD COMP C3 CH2	THD_C3_CH2						
0x3E	62	THD COMP C3 CH2	THD_C3_CH2						
0x3F	63	RESERVED	RESERVED						
0x40	64	ADC FIR FILTER	RESERVED			ADC_FILTER_SHAPE		RESERVED	
0x41	65	RESERVED	RESERVED						
0xC0	192	SOFT RESET	AO_ SOFT_RESET	PLL_ SOFT_RESET	RESERVED				PLL_ CLK_PHASE
0xC1	193	CLK SELECT	RESERVED	EN_ADC_CLK	SEL_PLL_IN		EN_PLL_CLKIN	SEL_SYSCLK_IN	RESERVED
0xC2	194	RESERVED	RESERVED						
0xC3	195	PLL SETTING 1	RESERVED					PLL_VCO_PDB	PLL_CP_PDB
0xC4	196	RESERVED	RESERVED						
0xC5	197	PLL SETTING 2	PLL_CLK_FB_DIV						
0xC6	198	PLL SETTING 2	PLL_CLK_FB_DIV						
0xC7	199	PLL SETTING 2	PLL_CLK_FB_DIV						
0xC8	200	PLL SETTING 3	PLL_CLK_IN_DIV						PLL_FB_DIV_ LOAD
0xC9	201	PLL SETTING 3	RESERVED		PLL_CLK_OUT_DIV			PLL_CLK_IN_DIV	
0xCA	202	PLL SETTING 3	PLL_REG_PDB		PLL_REG_BYP		RESERVED	PLL_CLK_ OUT_DIV_ PHASE_ENB	RESERVED
0xCB	203	PLL SETTING 4	RESERVED		PLL_DIG_RSTB	RESERVED			
0xCC	204	RESERVED	RESERVED						
0xE0	224	READ SYSTEM REGISTER 0	CLIP_FLAG_ CH2	CLIP_FLAG_ CH1	RESERVED	MODES		ADDR2	ADDR1	RESERVED
0xE1	225	CHIP ID	CHIP_ID						
0xE2 - 0xE6	226 - 230	RESERVED	RESERVED						
0xE7	231	TDM VALID READ	RESERVED		TDM_VALID	RESERVED			
0xE8	232	GPIO READBACK REGISTERS	RESERVED			GPIO5_ READBACK	GPIO4_ READBACK	GPIO3_ READBACK	GPIO2_ READBACK	GPIO1_ READBACK
0xE9 - 0xEC	233 - 236	RESERVED	RESERVED						
0xED	237	ADC PEAK CH1	ADC1_PEAK						

0xEE	238	ADC PEAK CH1	ADC1_PEAK
0xEF	239	ADC PEAK CH2	ADC2_PEAK
0xF0	240	ADC PEAK CH2	ADC2_PEAK

Table 18 - Register Map

Register Listings

Some RESERVED registers do not default to 0x00 and should not be modified for normal operation. If the value of the reserved registers is changed from the default state, it will be noted. Register defaults are set after CHIP_EN in enabled, or set high

Register 0: SYS CONFIG

Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	2'b11	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core except for the PLL Registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[6:5]	RESERVED	NA
[4]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled
[3]	ENABLE_SPDIF_ENCODE	Enables S/PDIF encoding clock. • 1'b0: S/PDIF clock disabled (default) • 1'b1: S/PDIF clock enabled
[2]	ENABLE_TDM_ENCODE	Enables I2S/TDM encoding clock. • 1'b0: I2S/TDM clock disabled • 1'b1: I2S/TDM clock enabled (default)
[1]	ENABLE_ADC_REG	Enables ADC Ch1 decimation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[0]	RESERVED	NA

Register 1: ADC CLOCK CONFIG1

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Enables BCK/FRAME ratio auto detect to determine TDM channels. • 1'b0: Disabled (default) • 1'b1: Auto detect BCK/FRAME ratio to determine the number of TDM channels
[6]	SELECT_ADC_HALF	Specifies whether to half SELECT_ADC_NUM divider. • 1'b0: Divide by SELECT_ADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_ADC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_ADC_NUM	Whole number divide value + 1 for CLK_ADC (SYS_CLK/divide_value). • 5'd0: Whole number divide value + 1 = 1 • 5'd1: Whole number divide value + 1 = 2 • 5'd31: Whole number divide value + 1 = 32

Register 2: ADC CLOCK CONFIG2

Bits	[7]	[6:0]
Default	1'b0	6'd0

Bits	Mnemonic	Description
[7]	ADC_CLK_DIV2	Sets ADC clock rate • 1'b0: full-rate (default) • 1'b1: 1/2 rate
[6:0]	RESERVED	NA

Register 3: I2S/TDM MASTER CLK CONFIG

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	SELECT_I2S_TDM_HALF	Specifies whether to half SELECT_I2S_TDM_NUM divider. • 1'b0: Divide by SELECT_I2S_TDM_NUM + 1 (default) • 1'b1: Divide by half of SELECT_I2S_TDM_NUM + 1 Note: Can only produce half of an odd number divide
[6:0]	SELECT_I2S_TDM_NUM	Whole number divide value + 1 for I2S/TDM master encoding clock (SYS_CLK/divide_value). • 7'd0: Whole number divide value + 1 = 1 (default) • 7'd1: Whole number divide value + 1 = 2 • 7'd127: Whole number divide value + 1 = 128

Register 4: I2S/TDM MASTER MODE CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'd0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	MASTER_BCK_DIV1	When enabled, master BCK is I2S/TDM master encoding clock. Otherwise, BCK is less than or equal to (I2S/TDM master encoding clock)/2 (unless when ***ENABLE_2X_MODE***is set). • 1'b0: BCK is not I2S/TDM master encoding clock (default) • 1'b1: BCK is I2S/TDM master encoding clock
[6]	MASTER_WS_IDLE	Sets the value of master WS when WS is idle. • 1'b0: WS is 0 when idle (default) • 1'b1: WS is 1 when idle
[5:4]	MASTER_FRAME_LENGTH	Selects the bit length in each I2S/TDM channel in master mode. • 2'd0: 32 bit (default) • 2'd2: 16 bit • others: Reserved
[3]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[2]	MASTER_BCK_INVERT	Inverts master BCK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[0]	MASTER_MODE_ENABLE	Enables I2S/TDM master mode and generates master BCK and master WS. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 5: TDM CONFIG1

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	TDM_BIT_DELAY	Indicates the MSB-2 position of the data from the frame start. Valid from 5'd0 to 5'd31 • 5'd0: Minimum • 5'd31: Maximum
[2]	TDM_VALID_EDGE	Sets on which WS edge the frame starts. • 1'b0: Frame starts on posedge of WS • 1'b1: Frame starts on negedge of WS (default)
[1]	TDM_LJ	Sets left-justified mode. • 1'b0: No left-justified (default) • 1'b1: Left-justified
[0]	TDM_LENGTH	Sets data length in each channel. • 1'b0: 32 bits (default) • 1'b1: 16 bits

Register 6: TDM CONFIG2

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	MASTER_WS_SCALE	In I2S/TDM master mode, tunes master BCK/WS ratio by scaling master WS. It allows more TDM slots in a fixed frame. • 3'd0: No scale (default) • 3'd1: Scale down WS by 2 • 3'd2: Scale down WS by 4 • 3'd3: Scale down WS by 8 • 3'd4: Scale down WS by 16 • others: Reserved
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 7: TDM SLOT CONFIG CH1

Bits	[7:6]	[5]	[4:0]
Default	2'b00	1'b0	5'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	SLAVE_BCK_INVERT	SLAVE BCK invert enable. • 1'b0: Non-inverted (default) • 1'b1: Invert BCK input
[4:0]	TDM_SLOT_SEL_CH1	Selects which TDM channel slot is filled by ADC Ch1 data. • 5'd0: Slot 1 (default) • 5'd1: Slot 2 • 5'd31: Slot 32

Register 8: TDM SLOT CONFIG CH2

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	TDM_SLOT_SEL_CH2	Selects which TDM channel slot is filled by ADC Ch2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 11-9: RESERVED

Register 12: INTERRUPT

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'b00	1'b0	1'b0	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	INTERRUPT_CLEAR_CH2_CLIP_DETECTION	Clears the clip detection interrupt of ADC Ch2 • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[4]	INTERRUPT_CLEAR_CH1_CLIP_DETECTION	Clears the clip detection interrupt of ADC Ch1 • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[3:2]	RESERVED	NA
[1]	INTERRUPT_MASK_CH2_CLIP_DETECTION	Masks the clip detection interrupt of ADC Ch2 • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted
[0]	INTERRUPT_MASK_CH1_CLIP_DETECTION	Masks the clip detection interrupt of ADC Ch1 • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted

Register 17-13: SPDIF CONFIG

Bits	[39:0]
Default	40'd0

Bits	Mnemonic	Description
[39:0]	SPDIF_CS	Configures S/PDIF sub-code bits.

Register 25-18: RESERVED

GPIO Registers

Register 26: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd2	4'd2

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output (default) • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 clip interrupt - output • 4'd6:Ch2 clip interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: RESERVED • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO1_CFG	Configure GPIO1 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output (default) • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 clip interrupt - output • 4'd6:Ch2 clip interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: RESERVED • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 27: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd2

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 clip interrupt - output • 4'd6:Ch2 clip interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: RESERVED • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO3_CFG	Configure GPIO3 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output (default) • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 clip interrupt - output • 4'd6:Ch2 clip interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: RESERVED • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 28: GPIO5 CONFIG

Bits	[7]	[6:4]	[3:0]
Default	1'b0	1'b0	4'd0

Bits	Mnemonic	Description
[7]	GPIO5_READ	GPIO5 readback enable. • 1'b0: GPIO5 readback disabled (default) • 1'b1: Allows readback of GPIO5 input
[6:4]	RESERVED	NA
[3:0]	GPIO5_CFG	Configure GPIO5 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 clip interrupt - output • 4'd6:Ch2 clip interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: RESERVED • 4’d13: CLK_ADC – output • 4’d14: Output 0 – output • 4’d15: Output 1 – output

Register 31-29: GPIO CONFIGS

Bits	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[23]	GPIO4_READ	GPIO 4 readback enable. • 1'b0: GPIO4 readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[22]	GPIO3_READ	GPIO 3 readback enable. • 1'b0: GPIO3 readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[21]	GPIO2_READ	GPIO 2 readback enable. • 1'b0: GPIO2 readback disabled (default) • 1'b1: Allows readback of GPIO2 input
[20]	GPIO1_READ	GPIO 1 readback enable. • 1'b0: GPIO1 readback disabled (default) • 1'b1: Allows readback of GPIO1 input
[19]	INVERT_GPIO5	GPIO5 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO5 output
[18]	INVERT_GPIO4	GPIO4 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO4 output
[17]	INVERT_GPIO3	GPIO3 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO3 output
[16]	INVERT_GPIO2	GPIO2 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO2 output
[15]	INVERT_GPIO1	GPIO1 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO1 output

[14]	GPIO5_WK_EN	GPIO5 weak keeper enable. • 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[13]	GPIO4_WK_EN	GPIO4 weak keeper enable. • 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[12]	GPIO3_WK_EN	GPIO3 weak keeper enable. • 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[11]	GPIO2_WK_EN	GPIO2 weak keeper enable. • 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[10]	GPIO1_WK_EN	GPIO1 weak keeper enable. • 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled
[9]	GPIO5_SDB	GPIO5 input enable. • 1'b0: GPIO5 input disabled (default) • 1'b1: GPIO5 input enabled
[8]	GPIO4_SDB	GPIO4 input enable. • 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled
[7]	GPIO3_SDB	GPIO3 input enable. • 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled
[6]	GPIO2_SDB	GPIO2 input enable. • 1'b0: GPIO2 input disabled • 1'b1: GPIO2 input enabled (default)
[5]	GPIO1_SDB	GPIO1 input enable. • 1'b0: GPIO1 input disabled • 1'b1: GPIO1 input enabled (default)
[4]	GPIO5_OE	GPIO5 output enable. • 1'b0: Tristate GPIO5 output (default) • 1'b1: GPIO5 output enabled
[3]	GPIO4_OE	GPIO4 output enable. • 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled

[2]	GPIO3_OE	GPIO3 output enable. • 1'b0: Tristate GPIO3 output • 1'b1: GPIO3 output enabled (default)
[1]	GPIO2_OE	GPIO2 output enable. • 1'b0: Tristate GPIO2 output • 1'b1: GPIO2 output enabled (default)
[0]	GPIO1_OE	GPIO1 output enable. • 1'b0: Tristate GPIO1 output • 1'b1: GPIO1 output enabled(default)

Register 32: PWM1 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd0: Minimum • 8'd255: Maximum

Register 34-33: PWM1 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Minimum • 16'hFFFF: Maximum $$frequency\ (Hz) = \frac{SYS_CLK}{PWM1_FREQ + 1}$$ $$Duty\ Cycle\ (\%) = \left(1 - \frac{(PWM1_FREQ + 1) - PWM1_COUNT}{PWM1_FREQ + 1}\right) \times 100$$

Register 35: PWM2 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd0: Minimum • 8'd255: Maximum

Register 37-36: PWM2 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Minimum • 16'hFFFF: Maximum $frequency\ [Hz] = \frac{SYS_CLK}{PWM2_FREQ + 1}$ $Duty\ Cycle\ [\%] = \left(1 - \frac{(PWM2_FREQ+1) - PWM2_COUNT}{PWM2_FREQ+1}\right) \times 100$

Register 38: PWM3 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd0: Minimum • 8'd255: Maximum

Register 40-39: PWM3 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Minimum • 16'hFFFF: Maximum $frequency\ [Hz] = \frac{SYS_CLK}{PWM3_FREQ + 1}$ $Duty\ Cycle\ [\%] = \left(1 - \frac{(PWM3_FREQ + 1) - PWM3_COUNT}{PWM3_FREQ + 1}\right) \times 100$

ADC Registers

Register 41: ADC DATAPATH CONTROL

Bits	[7]	[6]	[5]	[4:2]	[1]	[0]
Default	1'b1	1'b0	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	ADC_BYPASS_FIR2X	Dfir_2x bypass control. • 1'b0: Non-bypass (default) • 1'b1: Bypass Dfir_2x
[5]	ADC_BYPASS_FIR4X	Dfir_4x bypass control. • 1'b0: Non-bypass (default) • 1'b1: Bypass Dfir_4x
[4:2]	RESERVED	NA
[1]	CH1_AVR	Use (CH1+CH2)/2 as CH1 data. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	MONO_MODE	Mute CH2 decimation path. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 42: ADC DC BLOCKING AND SCALE CONFIG

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	2'd0	2'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	ADC_DATA_SCALE_CH2	ADC CH2 Digital data gain. • 2'd0: 0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB
[5:4]	ADC_DATA_SCALE_CH1	ADC CH1 Digital data gain. • 2'd0: 0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB
[3]	ADC_SELECT_DC_BLOCKING_CH2	Controls DC blocking filter output for decimation path CH2. • 1'b0: Bypass DC blocking filter output for decimation path CH2 (default) • 1'b1: Use DC blocking filter output for decimation path CH2
[2]	ADC_SELECT_DC_BLOCKING_CH1	Controls DC blocking filter output for decimation path CH1. • 1'b0: Bypass DC blocking filter output for decimation path CH1 (default) • 1'b1: Use DC blocking filter output for decimation path CH1
[1]	ADC_ENABLE_DC_BLOCKING_CH2	CH2 DC blocking filter control. • 1'b0: Disabled (default) • 1'b1: Enable DC blocking filter for CH2.
[0]	ADC_ENABLE_DC_BLOCKING_CH1	CH1 DC blocking filter enable. • 1'b0: Disabled (default) • 1'b1: Enable DC blocking filter for CH1.

Register 43: ADC PEAK DETECTOR CONFIG

Bits	[7]	[6:2]	[1]	[0]
Default	1'b0	5'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC_LOCK_PEAK	Locks the stored value of the peak detectors (CH1/2) for reading back. • 1'b0: Stored value is allowed to update (default) • 1'b1: Stored value is locked
[6:2]	ADC_DECAY_RATE	Sets the speed at which the stored value of the peak detector will decay when the input signal is below the stored value. • 5'd0: Instant decay (default) • 5'd63: Slowest decay
[1]	ADC_ENABLE_PEAK_DETECT_CH2	Enables the ADC CH2 signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_ENABLE_PEAK_DETECT_CH1	Enables the ADC CH1 signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 44: ADC CH1 PEAK DETECTOR LEVEL

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	ADC_CLIP_LEVEL_CH1	Threshold value of the CH1 clip detector. Valid from 8'hff (0dB) to 8'h01 (-48dB). • 8'h01 (-48dB): Minimum • 8'hFF (0dB): Maximum

Register 45: ADC CH2 PEAK DETECTOR LEVEL

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	ADC_CLIP_LEVEL_CH2	Threshold value of the CH2 clip detector. Valid from 8'hff (0dB) to 8'h01 (-48dB). • 8'h01 (-48dB): Minimum • 8'hFF (0dB): Maximum

Register 47-46: ADC CH1 DC OFFSET

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	ADC_CH1_DC_OFFSET	ADC CH1 DC offset. Signed. Shift right 1 bit corresponds to -6dB. • Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-114dB). • Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-114dB). • 16'h0000: zero offset

Register 49-48: ADC CH2 DC OFFSET

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	ADC_CH2_DC_OFFSET	ADC CH1 signed DC offset. Shift right 1 bit corresponds to -6dB. • Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-114dB). • Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-114dB). • 16'h0000: zero offset

Register 51-50: ADC CH1 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC_CH1_VOLUME	Next desired ADC CH1 signed volume coefficient. Shift right 1 bit corresponds to -6dB. • 16'h0000: Mute • 16'h0001 (-90dB): Minimum • 16h7FFF (0dB): Maximum (default) Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume.

Register 53-52: ADC CH2 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC_CH2_VOLUME	Next desired ADC CH2 signed volume coefficient. Shift right 1 bit corresponds to -6dB. • 16'h0000: Mute • 16'h0001 (-90dB): Minimum • 16h7FFF (0dB): Maximum (default) Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume.

Register 54: ADC VOLUME RATE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	ADC_VOLUME_RATE	Value by which the old coefficient value is incremented/decremented to reach the new coefficient. • 8'd0: Instant (default) • 8'd1: Slowest ramp rate • 8'd255: Fastest ramp rate

Register 56-55: THD COMP C2 CH1

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C2_CH1	A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 58-57: THD COMP C3 CH1

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C3_CH1	A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 60-59: THD COMP C2 CH2

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C2_CH2	A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 62-61: THD COMP C3 CH2

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	THD_C3_CH2	A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion. $$output = x + c2 * x^2 + c3 * x^3$$

Register 63: RESERVED

Register 64: ADC FIR FILTER

Bits	[7:5]	[4:2]	[1:0]
Default	3'd4	3'd0	2'b00

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:2]	ADC_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[1:0]	RESERVED	NA

Register 65: RESERVED

Synchronous Slave Interface (no clock required)

Register 192: SOFT RESET

Bits	[7]	[6]	[5:1]	[0]
Default	1'b0	1'b0	5'd0	1'b0

Bits	Mnemonic	Description
[7]	AO_SOFT_RESET	Performs soft reset to clocked registers. Includes registers 0 to 64 and readback registers. • 1'b0: Disabled (default) • 1'b1: Enable
[6]	PLL_SOFT_RESET	Performs soft reset to the clock not required registers including registers 192-203. • 1'b0: Disabled (default) • 1'b1: Enable
[5:1]	RESERVED	NA
[0]	PLL_CLK_PHASE	Inverts the phase of the digital/analog ADC clock. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 193: CLK SELECT

Bits	[7]	[6]	[5:4]	[3]	[2:1]	[0]
Default	1'b0	1'b1	2'b10	1'b0	2'd0	1'b1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	EN_ADC_CLK	Enables analog ADC clock. • 1'b0: Disabled • 1'b1: Enabled (default)
[5:4]	SEL_PLL_IN	Selects PLL input clock source when EN_PLL_CLKIN is set. • 2'd0: ACLK1 • 2'd1: ACLK2 • 2'd2: BCK(default) • 2'd3: Reserved
[3]	EN_PLL_CLKIN	Allows SEL_PLL_IN to select PLL input clocks. • 1'b0: Disables SEL_PLL_IN (default) • 1'b1: Enables SEL_PLL_IN
[2:1]	SEL_SYSCLK_IN	Selects digital core and ADC clock source when EN_ANA_CLKIN is set. • 2'd0: ACLK1 (default) • 2'd1: ACLK2 • 2'd2: PLL

		• 2'd3: Reserved
[0]	RESERVED	NA

Register 194: RESERVED

Register 195: PLL SETTING 1

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'b111	3'b111	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	PLL_CP_BIAS_SEL	Sets the PLL Charge Pump BIAS current value: • **3'b011:4u (optimum setting, for normal operation)**
[4:2]	RESERVED	NA
[1]	PLL_VCO_PDB	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CP_PDB	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 196: RESERVED

Register 199-197: PLL SETTING2

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider. • 24'd0: Reserved • 24'dn: Divide by (2^25)/n

Register 202-200: PLL SETTING3

Bits	[23:22]	[21:20]	[19]	[18]	[17:14]	[13:10]	[9:1]	[0]
Default	2'b00	2'b00	1'b1	1'b0	4'd0	4'd0	9'd0	1'b0

Bits	Mnemonic	Description
[23:22]	PLL_REG_PDB	Power Down the PLL regulators. • 2'b00: Disables the PLL regulators • 2'b11: Enables the PLL regulators **(Normal Operation)** **Note: Other options not valid**
[21:20]	PLL_REG_BYP	Bypass mode of the PLL regulators. • 2'b00: **Normal Operation** • 2'b11: Bypass the PLL regulators **Note: Other options not valid**
[19]	RESERVED	NA
[18]	PLL_CLK_OUT_DIV_PHASE_ENB	• 1'b0: Locks the PLL clock output divider phase. (default) • 1'b1: Disabled
[17:14]	RESERVED	NA
[13:10]	PLL_CLK_OUT_DIV	Sets the Output Division (No) of the PLL. • 4'd0: Divide by 1 **(Normal starting value)** • 4'd1: Divide by 2 • 4'd3: Divide by 4 • 4'dn: Divide by (n + 1)
[9:1]	PLL_CLK_IN_DIV	Sets the Input Division (Ni) of the PLL. • 9'd0: Divide by 1 **(Normal starting value)** • 9'd1: Divide by 2 • 9'd3: Divide by 4 • 9'dn: Divide by (n + 1)
[0]	PLL_FB_DIV_LOAD	Load PLL_CLK_FB_DIV • Write 1'b1 then 1'b0 to load PLL_CLK_FB_DIV value

Register 203: PLL SETTING4

Bits	[7:6]	[5]	[4:0]
Default	2'd0	1'b0	5'b01001

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PLL_DIG_RSTB	Resets the Digital core of the PLL.
[4:0]	RESERVED	NA

Register 204: RESERVED

System Readback Registers

Register 224: READ SYSTEM REGISTER 0

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	CLIP_FLAG_CH2	ADC CH2 clip detection flag • 1'b0: Inactive • 1'b1: Active
[6]	CLIP_FLAG_CH1	ADC CH1 clip detection flag • 1'b0: Inactive • 1'b1: Active
[5]	RESERVED	NA
[4:3]	MODES	Chip mode readback. Based off MODE pin • 2'b00: I2C • 2'b11: SPI Note: All other values are invalid
[2]	ADDR1	Readback of ADDR1 pin
[1]	ADDR0	Readback of ADDR0 pin
[0]	RESERVED	NA

Register 225: CHIP ID

Bits	[7:0]
Default	8'h88

Bits	Mnemonic	Description
[7:0]	CHIP_ID	Readback Chip ID from ES9821

Register 229-227: RESERVED

Register 230: RESERVED

Register 231: TDM VALID READ

Bits	[7:6]	[5]	[4:0]
Default	-	-	-

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	TDM_VALID	TDM valid flag
[4:0]	RESERVED	NA

GPIO Readback Registers

Register 232: GPIO READBACK REGISTERS

Bits	[7:5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4]	GPIO5_READBACK	GPIO5 readback.
[3]	GPIO4_READBACK	GPIO4 readback.
[2]	GPIO3_READBACK	GPIO3 readback.
[1]	GPIO2_READBACK	GPIO2 readback.
[0]	GPIO1_READBACK	GPIO1 readback.

ADC Readback Registers

Register 236-233: RESERVED

Register 238-237: ADC PEAK CH1

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC1_PEAK	Ch1 detected signal peak value readback.

Register 240-239: ADC PEAK CH2

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC2_PEAK	Ch2 detected signal peak value readback

ES9821Q Reference Schematic (Hardware Mode)

See Hardware Mode **section for additional details on configuration for Hardware mode**

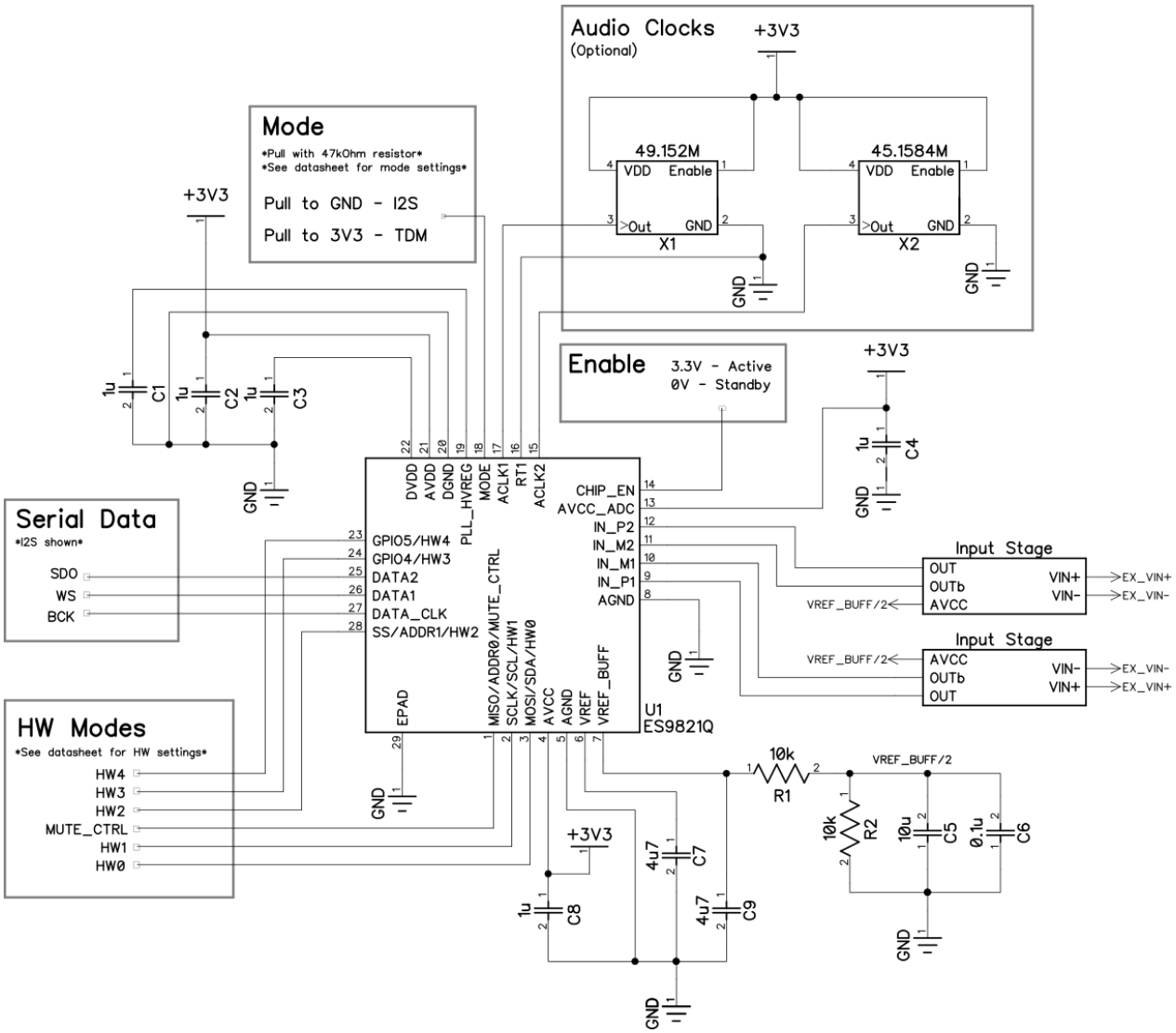


Figure 12 - ES9821Q Reference schematic for normal operation in Hardware (HW) mode

Schematic subject to change

Note 1: Pin 29 QFN Package Pad (EPAD) should be connected to DGND

Note 2: See Hardware mode section for additional details on configuration for Hardware mode

ES9821Q Reference Schematic (Software Mode)

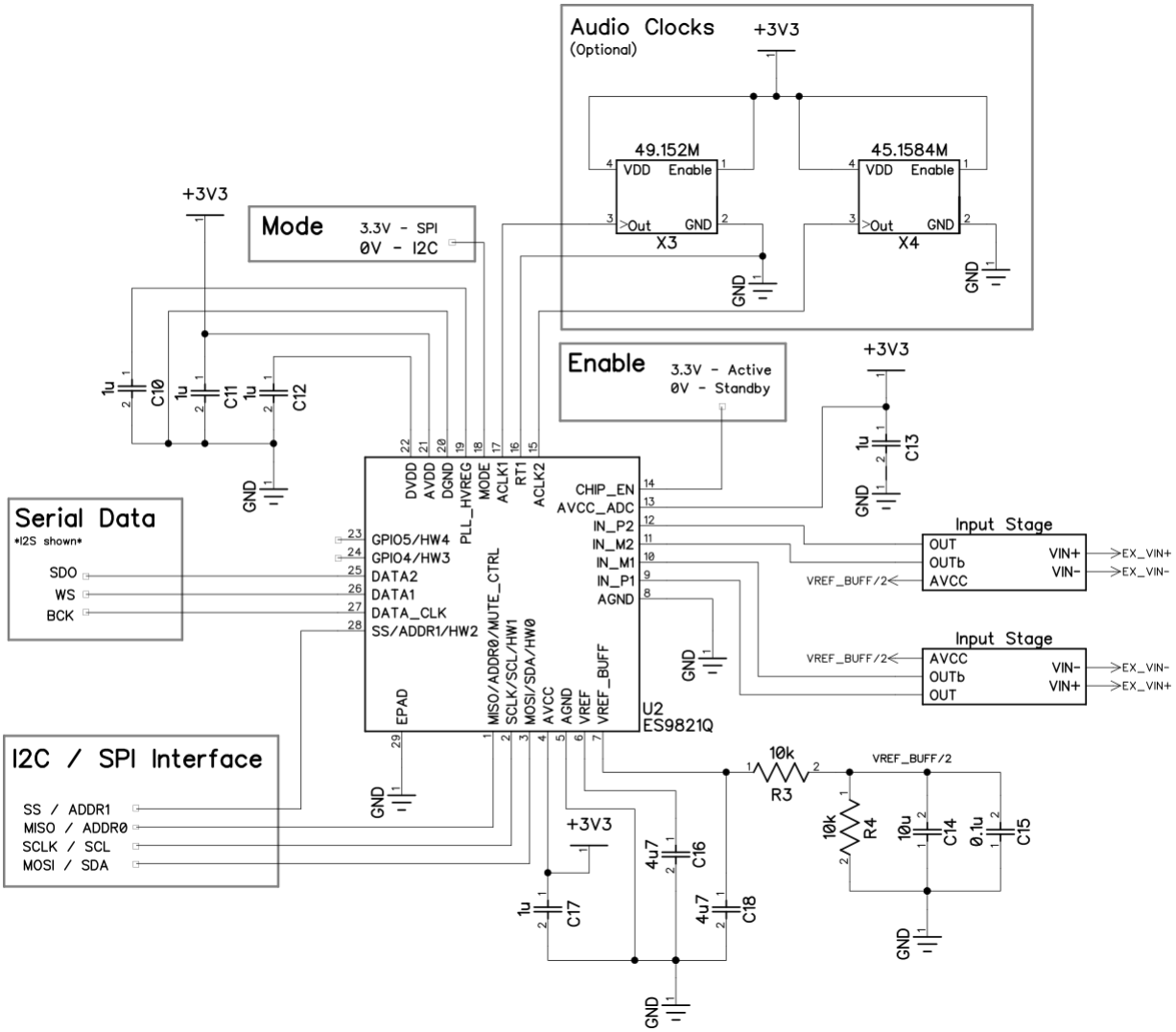
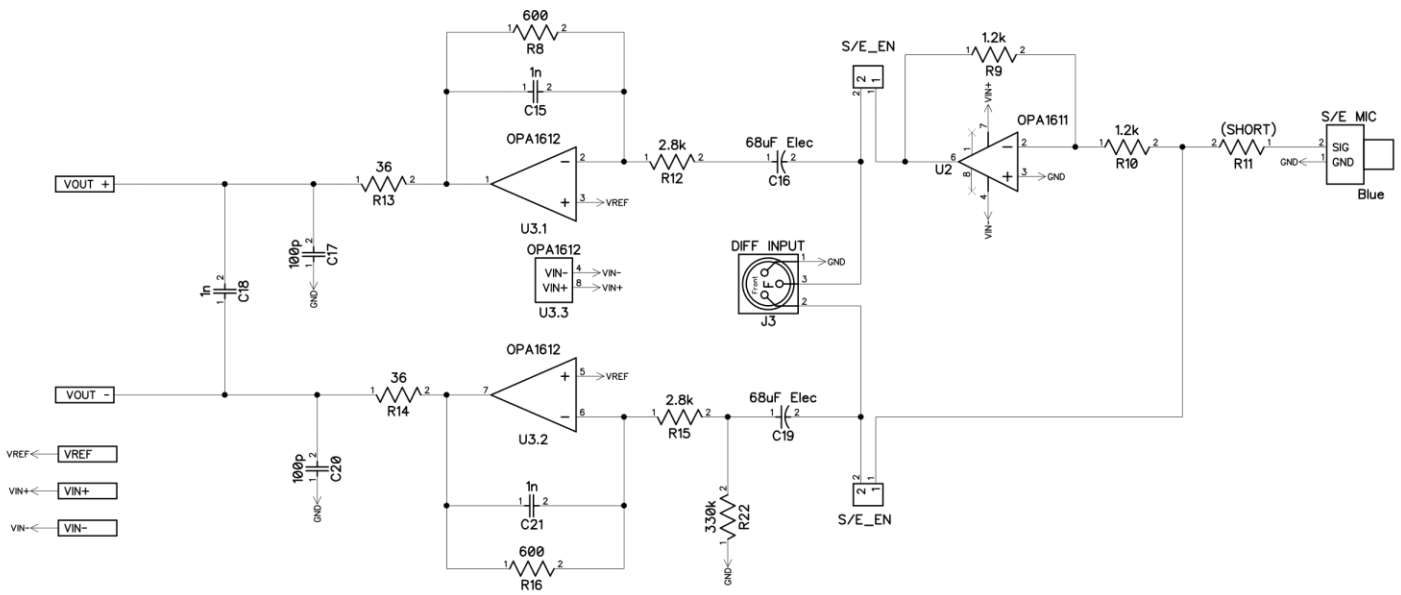


Figure 13 - ES9821Q Reference schematic for normal operation in Software (SW) mode

Schematic subject to change

Note 1: Pin 29 QFN Package Pad (EPAD) should be connected to DGND

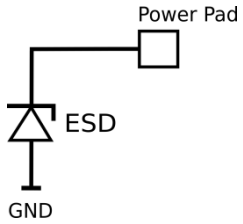
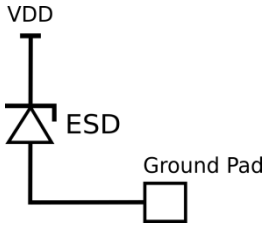
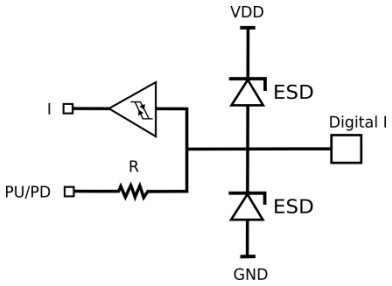
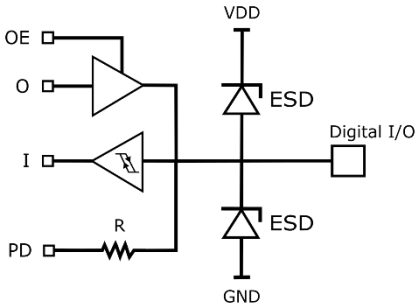
Note 2: Pullup resistors are required on the SCL/SDA pins if using the I2C interface



Note: All resistors are thin-film and all caps are COG/NPO unless otherwise specified

Figure 14 - Reference schematic ADC input stage for Single Ended (S/E) and differential input

Internal Pad Circuitry

Pin	Type	Pin Name	Equivalent Circuit
AVCC_ADC AVDD AVCC	Power	13 4 21	
AGND AGND DGND	Ground	5 8 19	
CHIP_EN	Reset	23	
MISO/ADDR0/MUTE_MCLK_CTRL SCLK/SCL/HW1 MOSI/SDA/HW0 MODE GPIO5/HW4 GPIO4/HW3 DATA2 DATA1 DATA_CLK SS/ADDR1/HW2	Digital I/O	1 2 3 18 23 24 25 26 27 28	

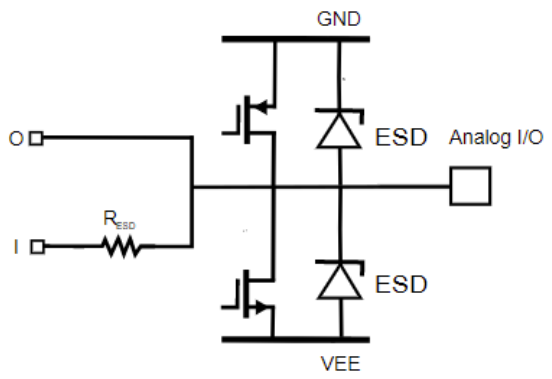
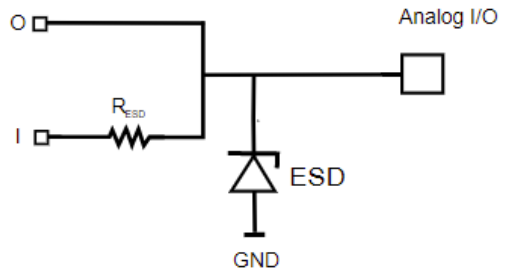
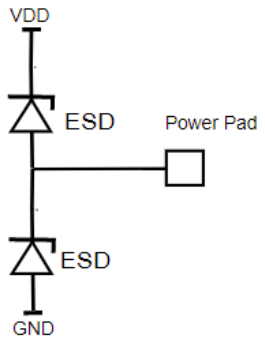
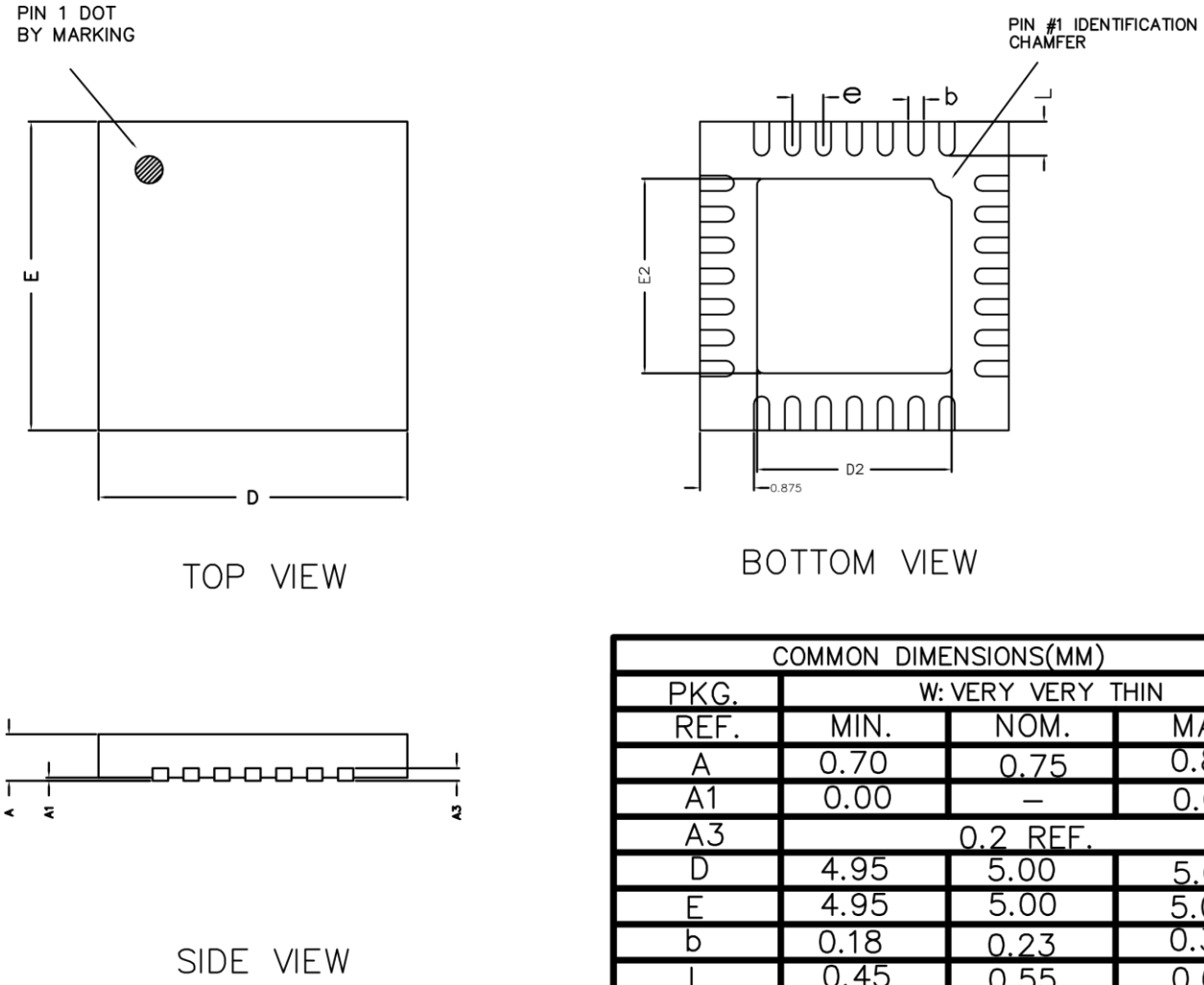
VREF VREF_BUF	Analog_IO_2XVDD	6 7	
IN_P1 IN_P2 IN_M1 IN_M2	Analog IO ADC	9 12 10 11	
DVDD	IO Power	22	

Table 19 - Internal pad circuitry

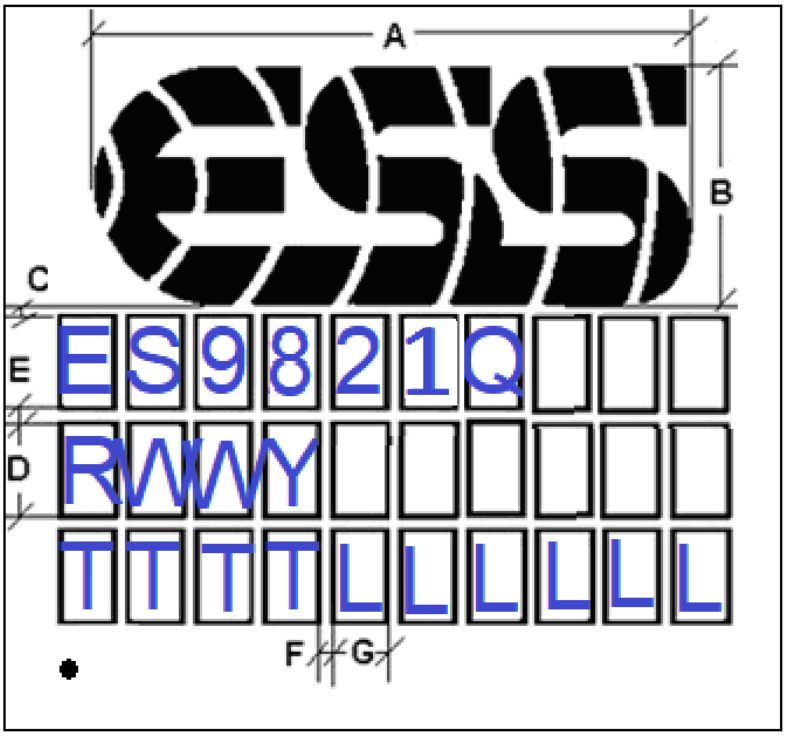
28 QFN Package Dimensions



COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.2 REF.		
D	4.95	5.00	5.05
E	4.95	5.00	5.05
b	0.18	0.23	0.30
L	0.45	0.55	0.65
D2	3.00	3.15	3.25
E2	3.00	3.15	3.25
e	0.5 BSC		

Figure 15 - 28 QFN package dimensions

28 QFN Top View Marking



	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

T	*Tracking number*
W	*Work week*
Y	*Last digit of year*
L	*Lot number*
R	*Silicon Revision*

Marking is subject to change. This drawing is not to scale.

Figure 16 - ES9821Q QFN Marking

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

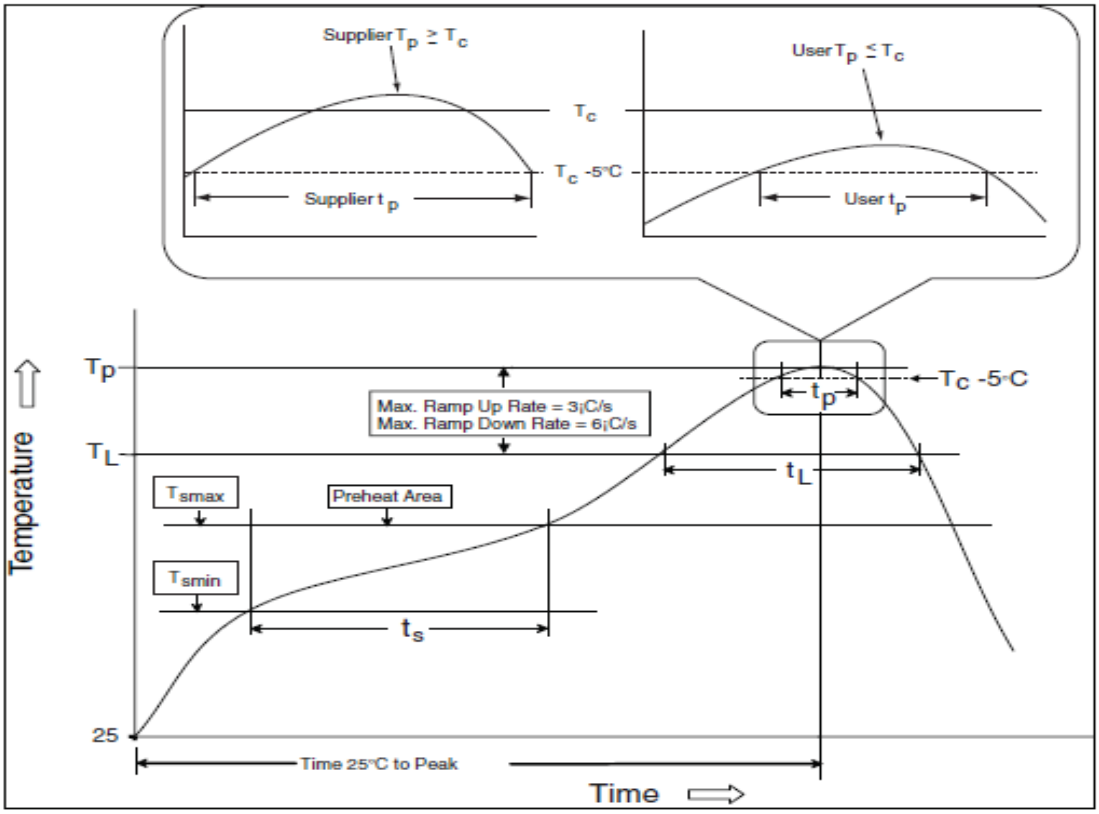


Figure 17 -IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see **Error! Reference source not found.**9	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 20 - RPC-1 Classification reflow profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug).If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 21 - RPC-2 Pb free classification temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9821Q	SABRE 32-bit 2 Channel ADC with built in digital filters, and multiple output formats	5mm x 5mm 28 QFN
ES9821QT* • **Inquire for availability**	ES9821Q with extended temperature range (-40 deg C to 105 deg C)	5mm x 5mm 28 QFN

Table 22 - Ordering information

Revision History

Current Version 0.2.1

Rev.	Date	Notes
0.1.3	Nov 5, 2021	Initial release
0.1.4	Dec 21, 2021	• Updated Register 42 descriptions for clarity • Updated HW/SW schematics with correct AVCC voltage
0.2.1	Sept, 2022	• Added HW modes 12-15 to Hardware Mode Pin Configurations • Reserved Register 12[6] & [2] • Unreserved Register 193[5:4] • Update Power Consumption numbers • Reserved Register 194 • Updated Register 224,225, 32-40, 4[7] • Added note to add pullup resistors for I2S software mode • Updated Performance Table values • Removed PU from Digital I/O equivalent circuit • Updated Register 202-200: PLL SETTING 3 [18:1] descriptions • Added Analog PLL section

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